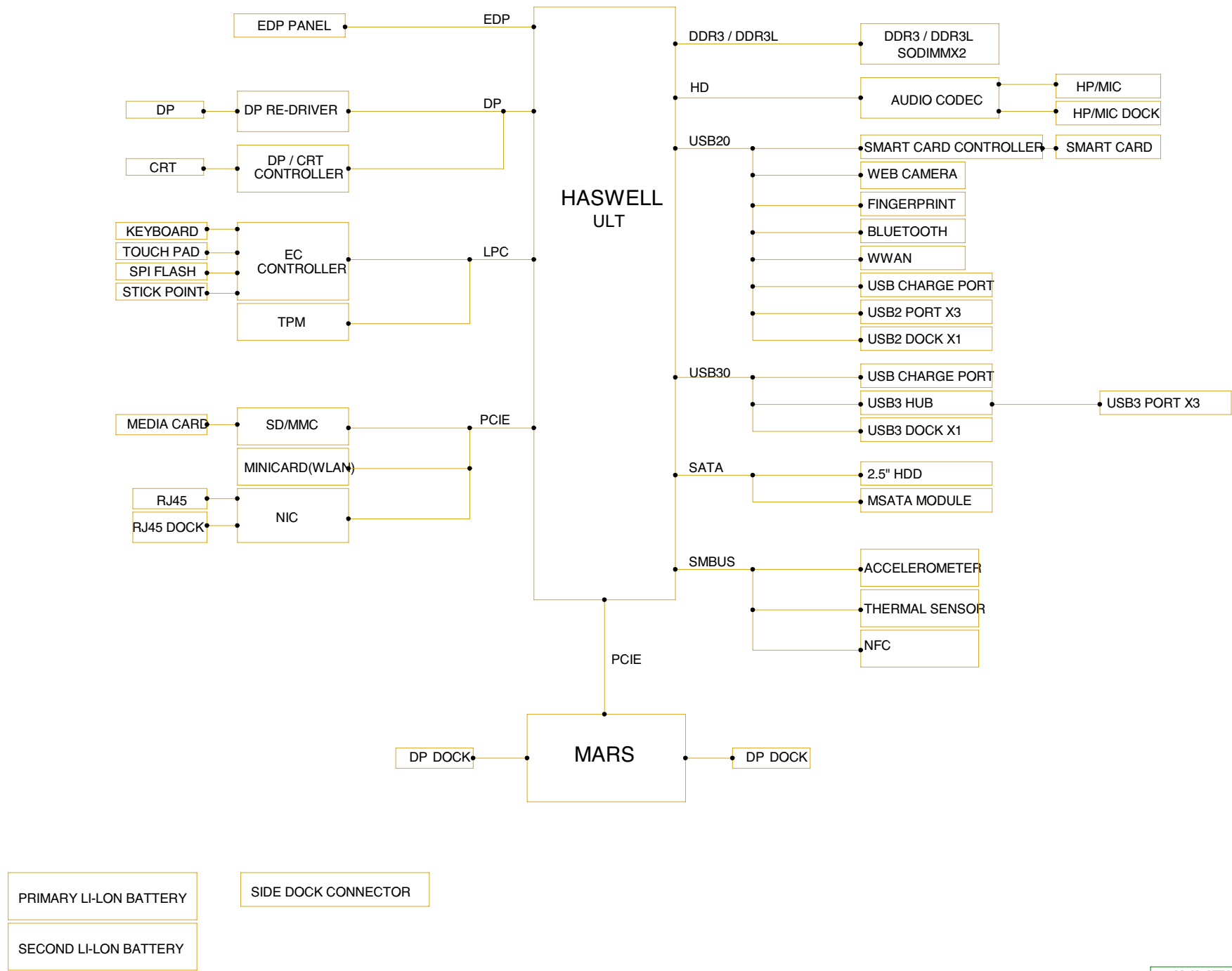


HSF Property:ROHS or Halogen-Free

2012.11.30

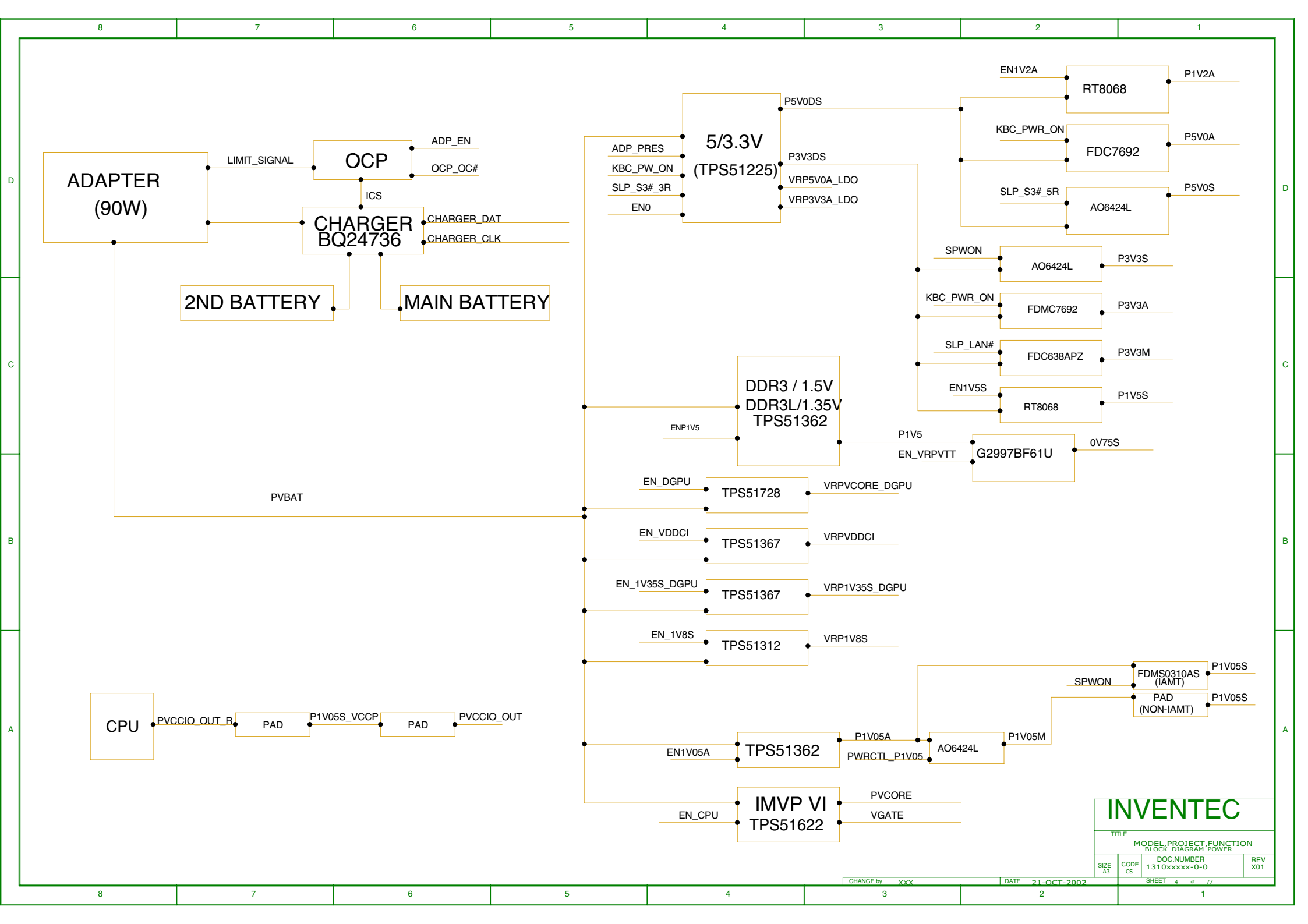
					<b>INVENTEC</b>					
DRAWER	EE	DATE	POWER	DATE						
	10X CHEN	2012/10/24	80AT CHEN	2012/10/24						
DESIGN CHECK	10X CHEN	2012/10/24	80AT CHEN	2012/10/24						
RESPONSIBLE	10X CHEN	2012/10/24	80AT CHEN	2012/10/24	TITLE	MODEL PROJECT FUNCTION				
	10X CHEN	2012/10/24	80AT CHEN	2012/10/24	COMET					
					CODE	DOC NUMBER			REV	X01
FILE NAME	COMET OS				SIZE	C5	1310XXXXXX-0-0			
PIN	42919100000 - XXXY				SHEET	d 77				



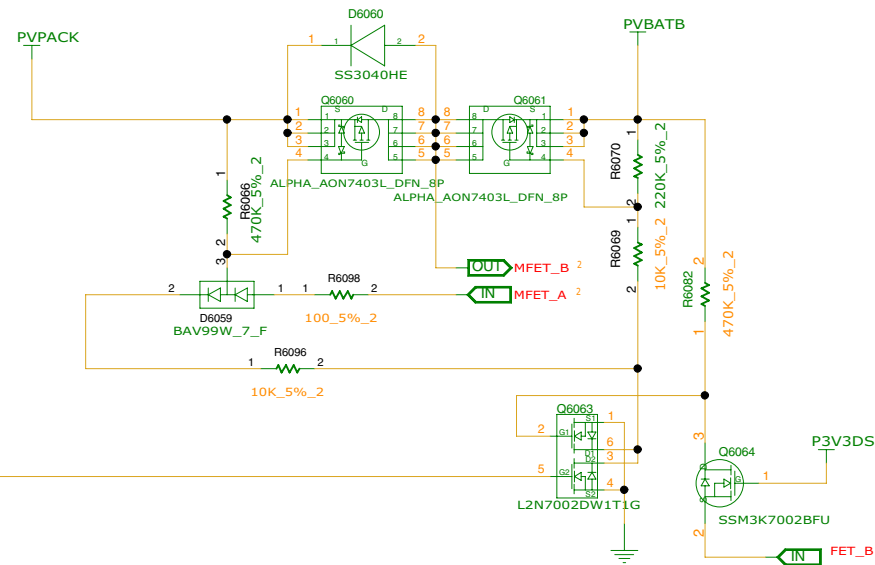
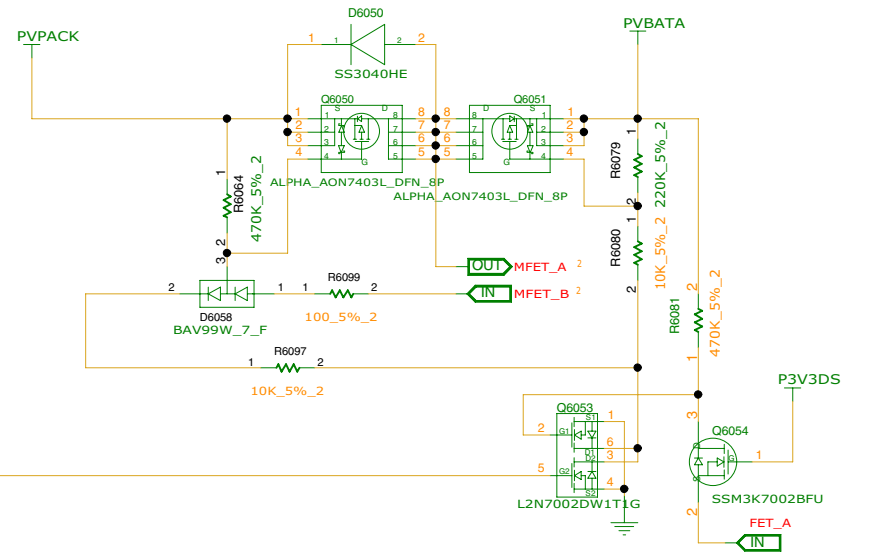
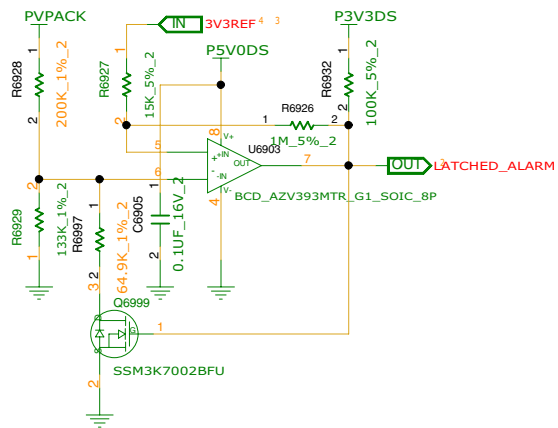
# TABLE OF CONTENTS

01.PROJECT NAME	26.XDP & ME CONN.	51.KBC, SPI
02.BLOCK DIAGRAM	27.HASWELL_1 (MISC,JTAG)	52.KEYBOARD
03.TABLE OF CONTENTS	28.HASWELL_2 (LPC,SPI,SMBUS,CLINK,PM)	53.TPM
04.POWER BLOCK DIAGRAM	29.HASWELL_3 (GPIO)	54.LAN
05.SYSTEM POWER(CHARGER)	30.HASWELL_4 (DP,EDP)	55.WLAN/BT SLOT
06.SYSTEM POWER(BATT SELECTOR)	31.HASWELL_5 (DDR)	56.WWAN SLOT, SIM SLOT
07.SYSTEM POWER(OCF)	32.HASWELL_6 (PCIE,USB)	57.DOCKING
08.SYSTEM POWER(P3V3A&P5V0A)	33.HASWELL_7 (RTC,AUDIO,SATA,JTAG)	58.B TO B CONN, POINT STICK CONN
09.P3V3A&P5V0A_CHG PORT	34.HASWELL_8 (CLK)	59.AUDIO CODEC
10.SYSTEM POWER(P1V5)	35.HASWELL_9 (POWER)	60.AUDIO JACK, MIC AMP.
11.SYSTEM POWER(P1V05_M)	36.HASWELL_10 (POWER)	61.CARD READER
12.SYSTEM POWER(P1V05S)	37.HASWELL_11 (GND)	62.BUTTON, LED
13.USB HUB POWER (P1V2A)	38.SYSTEM MEMORY (DIMM0)	63.SMART CARD DAUGHTER BOARD
14.SYSTEM POWER(PVCORE&PVAXG-1)	39.SYSTEM MEMORY (DIMM1)	64.CRT DB WTB CONN
15.SYSTEM POWER(PVCORE&PVAXG-2)	40.EMPTY	65.MIC DB
16.POWER SEQUENCE (SLEEP)	41.EMPTY	66.SCREW
17.DC JACK & BATTERT CONN.	42.DP TO VGA CONVERTER	67.EMPTY
18.HP_OCF	43.DISPLAY PORT	68.MARS-1
19.PVCORE_DGPU	44.LCM & WEBCAM CONN	69.MARS-2
20.PVDDCI	45.SATA HDD, MSATA	70.MARS-3
21.P1V35S_DGPU	46.USB HUB	71.MARS-4
22.P1V8S	47.USB3 PORTS	72.MARS-5
23.PVPCIE	48.USB & CRT DB	73.MARS-6
24.POWER (SEQUENCE)	49.FINGERPRINT READER, NFC	74.MARS-7
25.FAN & THERMAL	50.ACCELEMETER	75.MARS-8
		76.VRAM-1
		77.VRAM-2

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
TABLE OF CONTENTS			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 3 of 77			







LATCHED\_ALARM OUT

INVENTEC

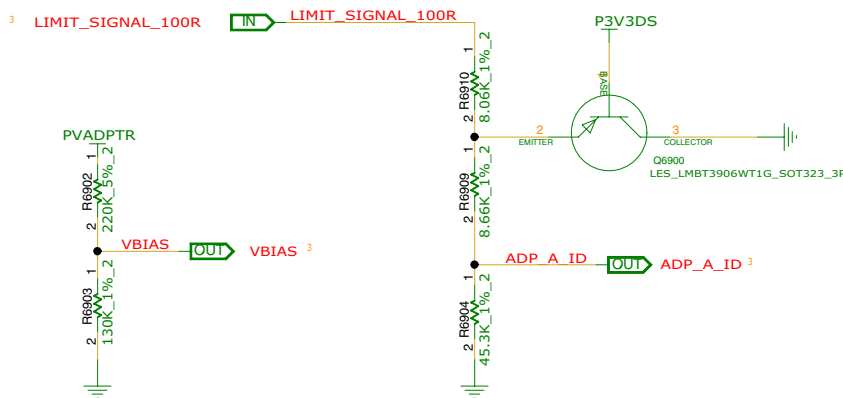
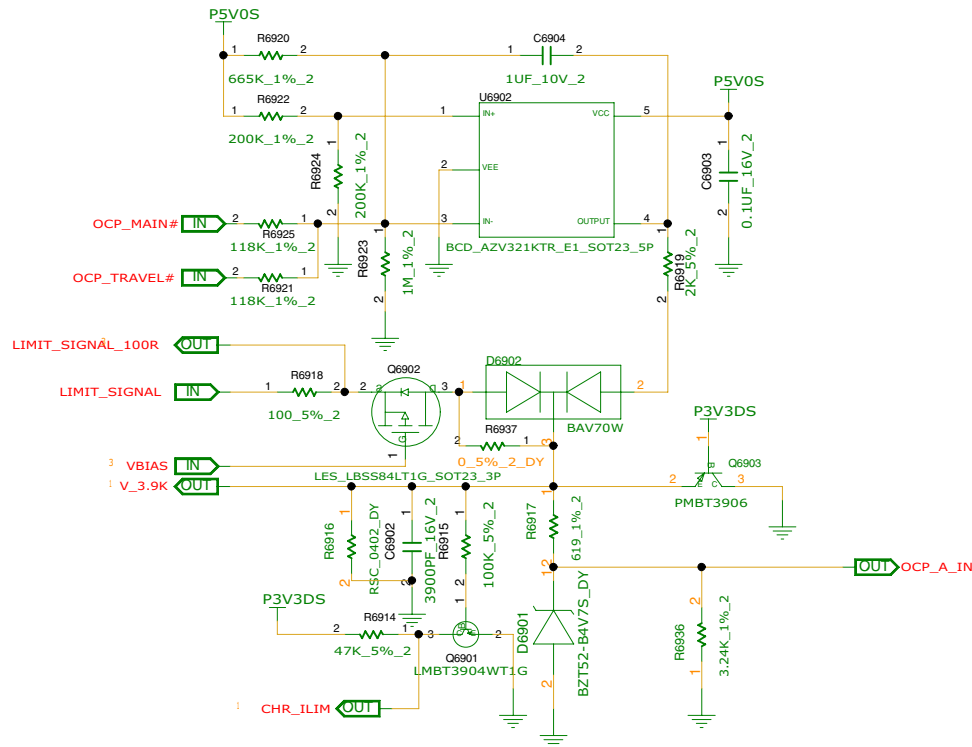
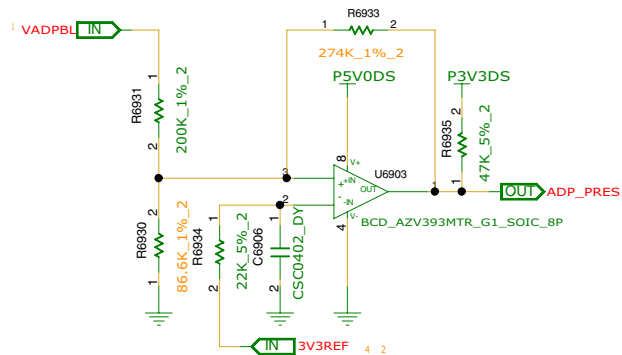
TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

DOC NUMBER  
1310xxxxx-0-0

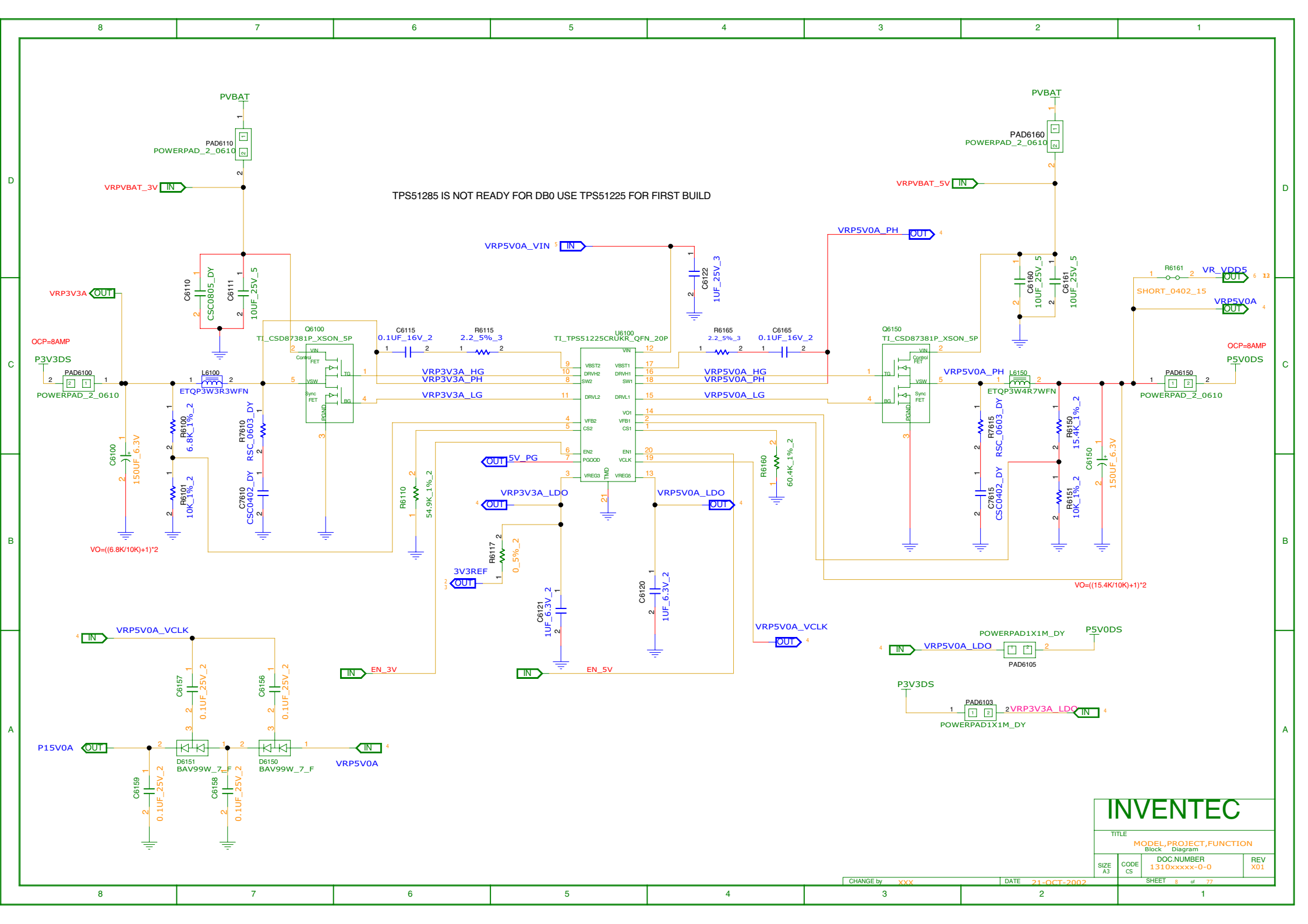
REV  
X01

CHANGE by XXX DATE 21-OCT-2002

SHEET 6 of 77



INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 7 of 77			

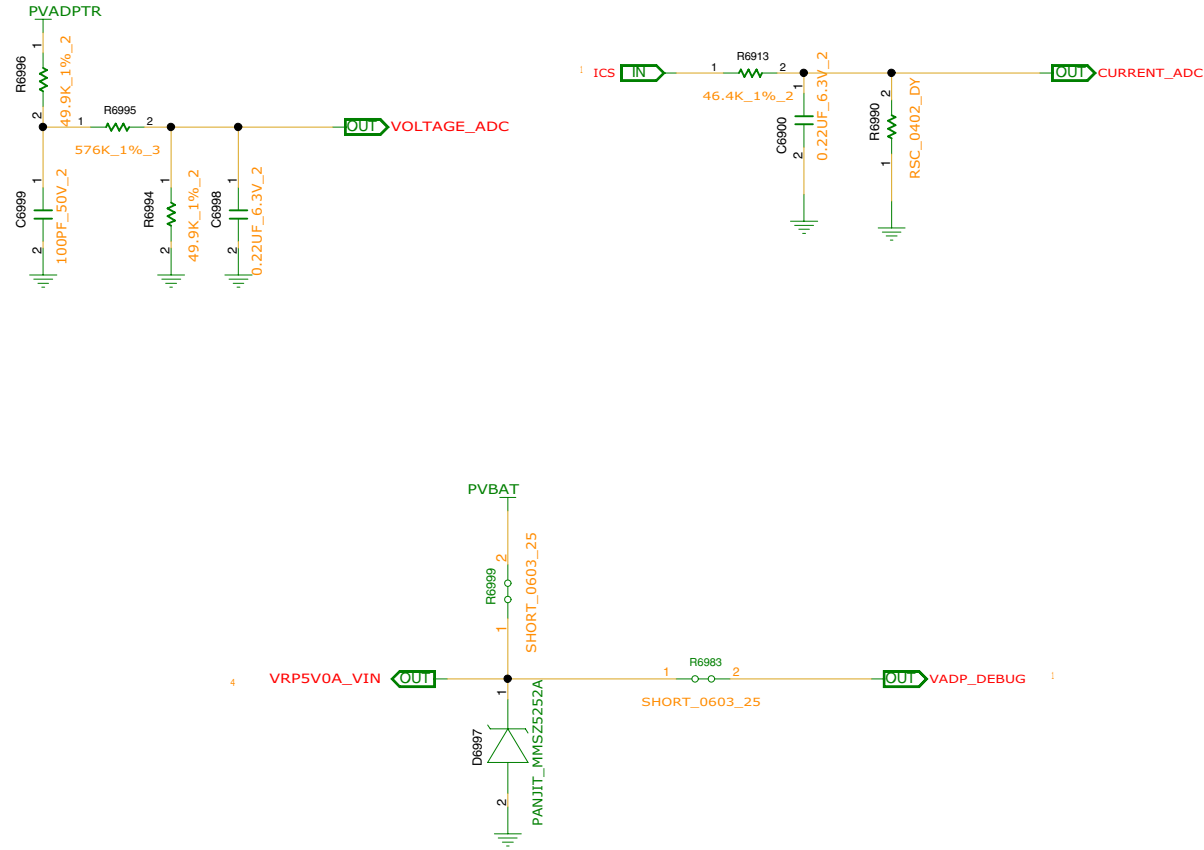


TPS51285 IS NOT READY FOR DB0 USE TPS51225 FOR FIRST BUILD

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01



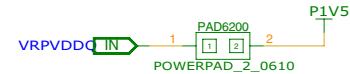
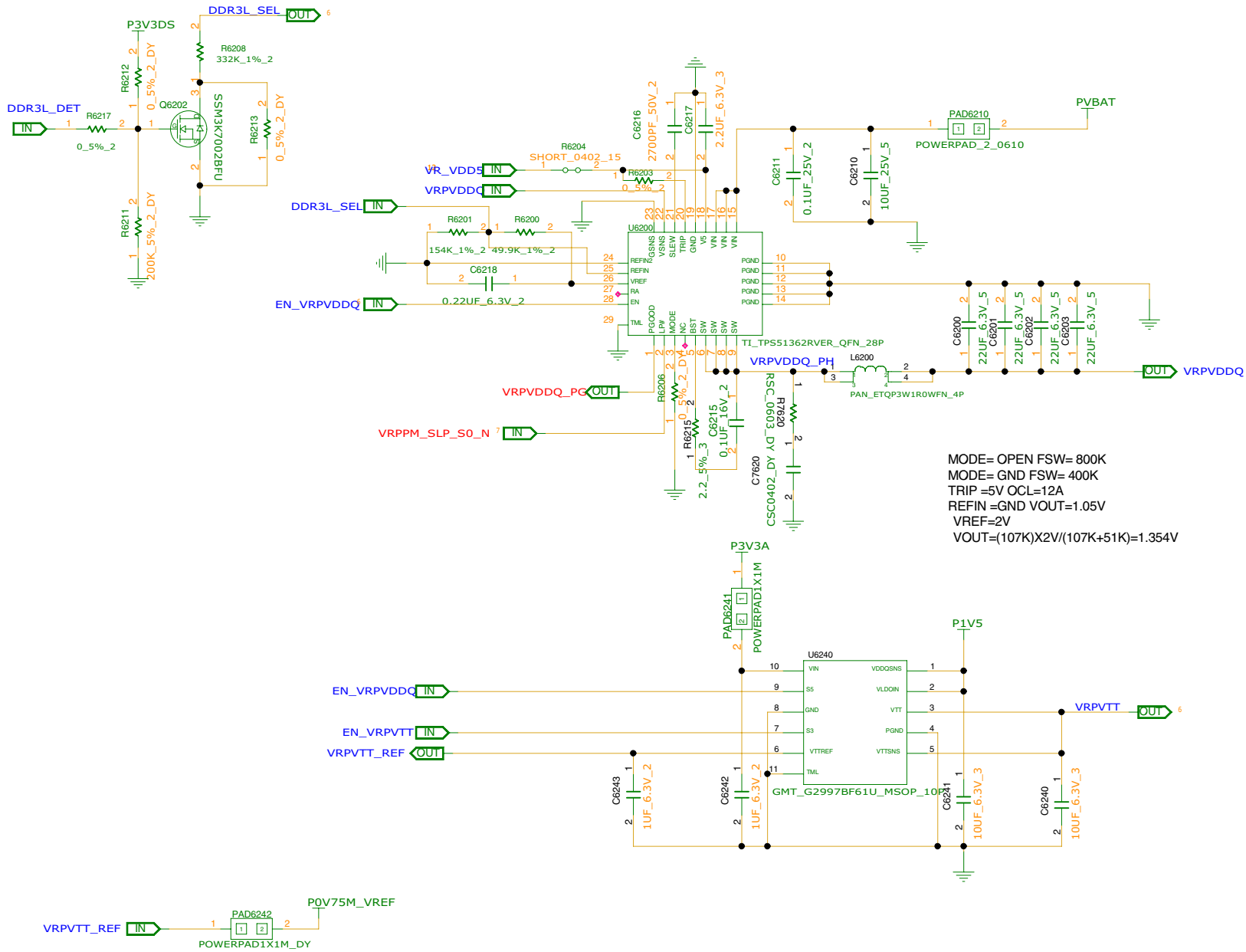


INVENTEC

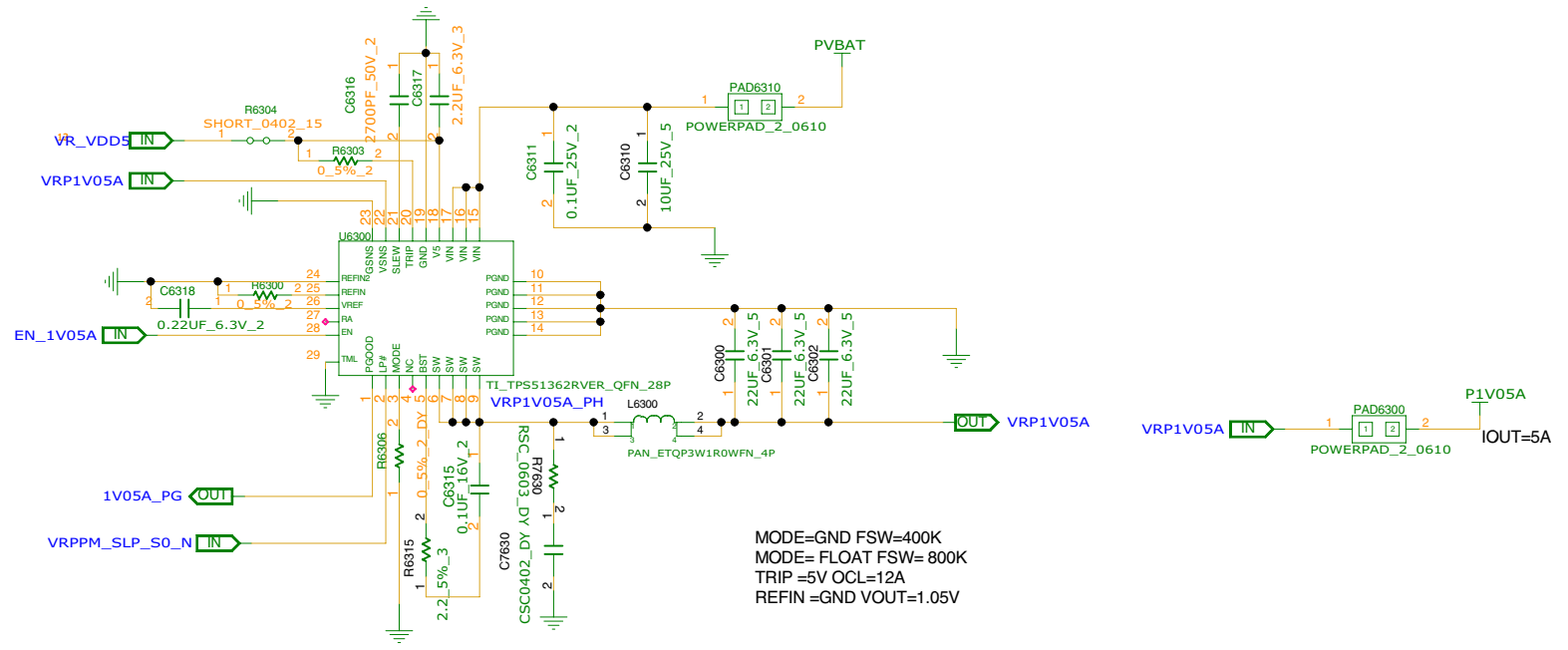
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX DATE 21-OCT-2002

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<b>INVENTEC</b>			
TITLE MODEL,PROJECT,FUNCTION			
DOC NUMBER 1310xxxxx-0-0			
SIZE A3	CODE CS	REV X01	
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 10 of 77			



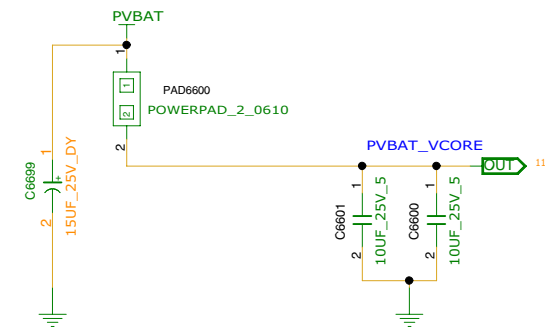
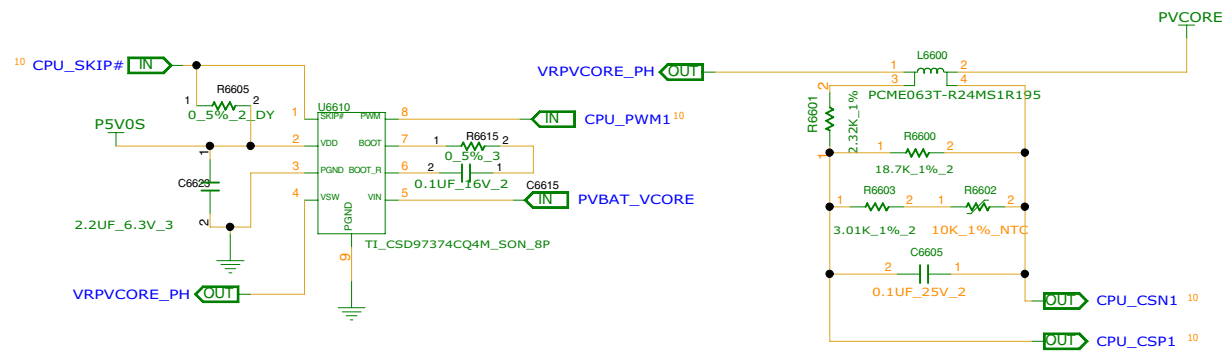
MODE=GND FSW=400K  
MODE= FLOAT FSW= 800K  
TRIP =5V OCL=12A  
REFIN =GND VOUT=1.05V

<b>INVENTEC</b>			
TITLE MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 11 of 77









# INVENTEC

TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
		SHEET 15 of 77	

CHANGE by	XXX	DATE	21-OCT-2002
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[illegible]

# INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block      Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET    16    of    77			









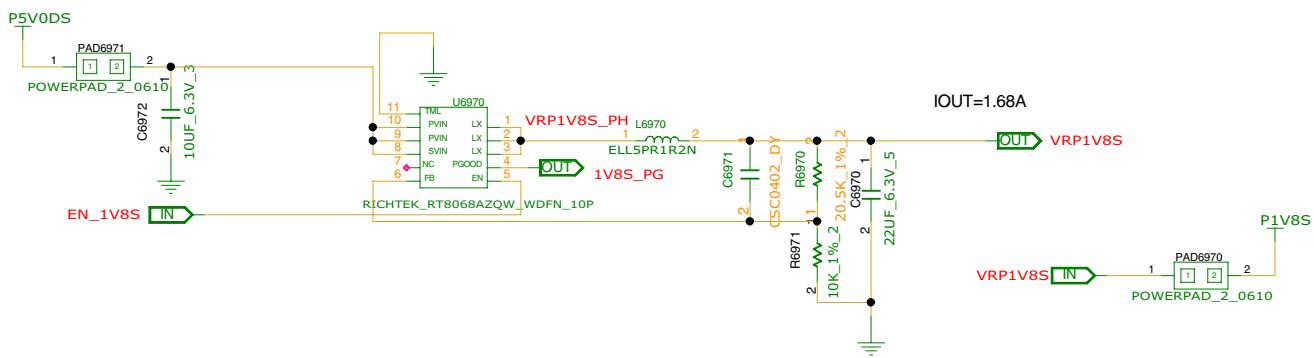
	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

EMPTY

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 20 of 77			

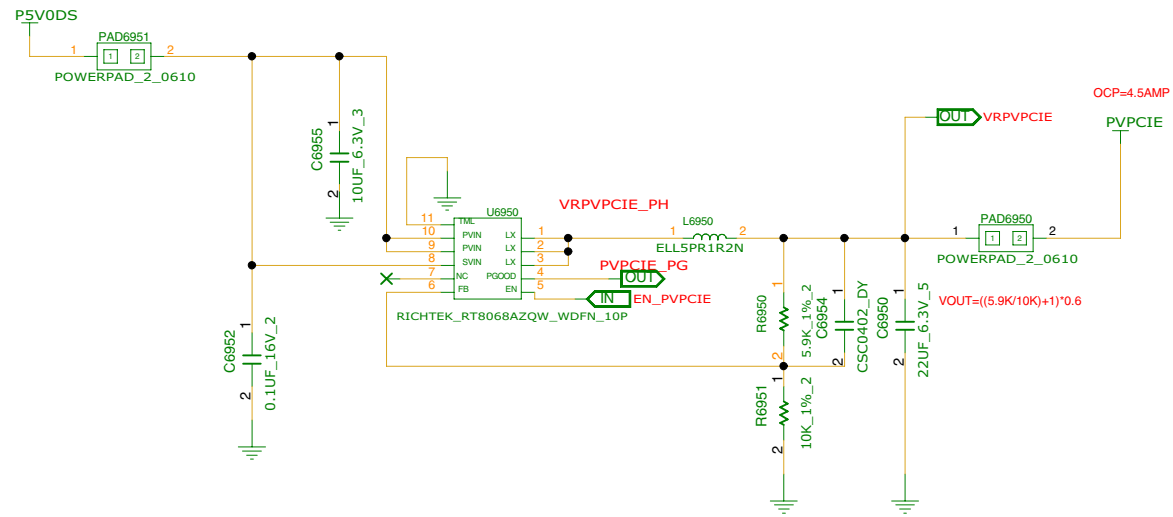




VREF=0.6V  
15K=1.5V  
10K=1.2V  
20.5K=1.83V  
MODE=FLOAT=SKIP MODE  
MODE=VIN=FCCM MODE

INVENTEC

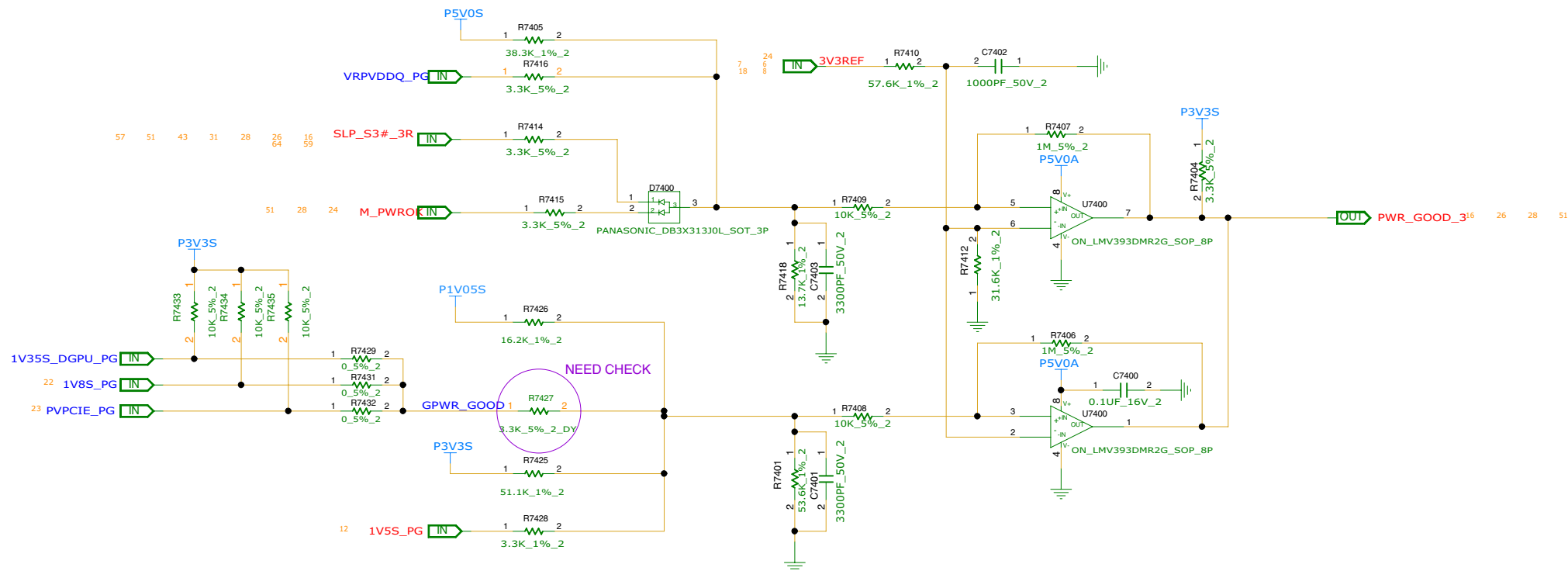
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01



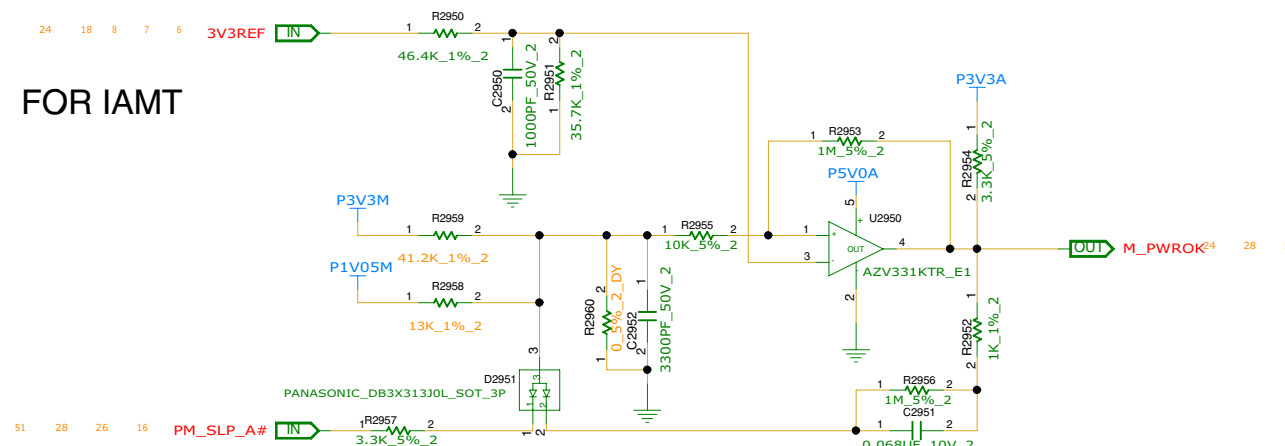
INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

# REFERENCE NUMER : 7400~7450



## FOR IAMT



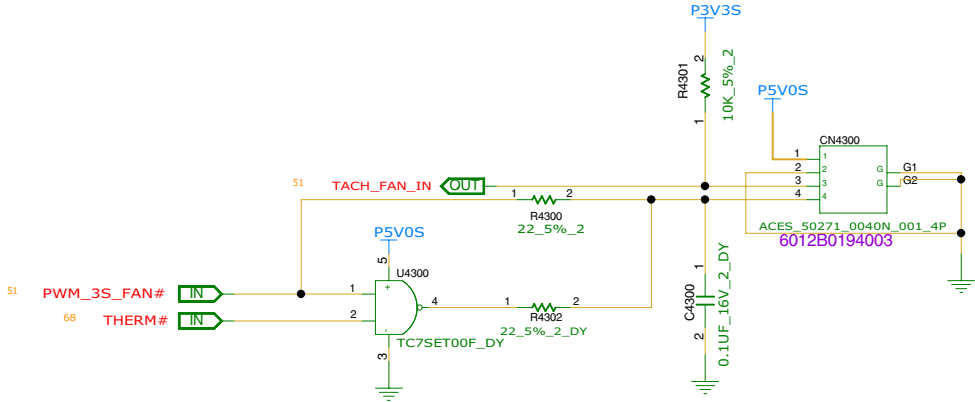
REFERENCE NUMER : 2950~2999

INVENTEC

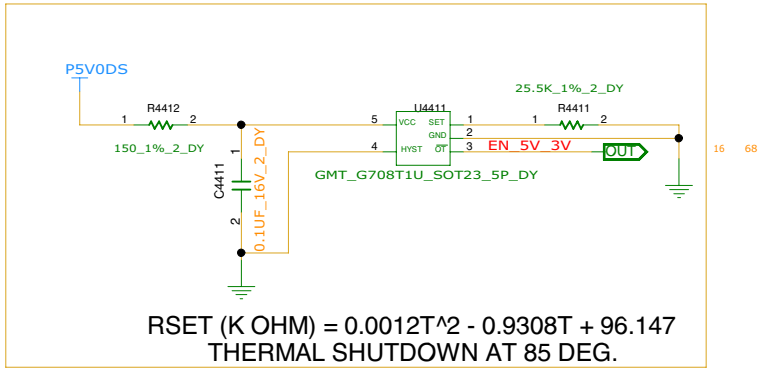
TITLE			
MODEL PROJECT FUNCTION POWER (SEQUENCE)			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 24 of 77			



REFERENCE NUMBER:4400~4349



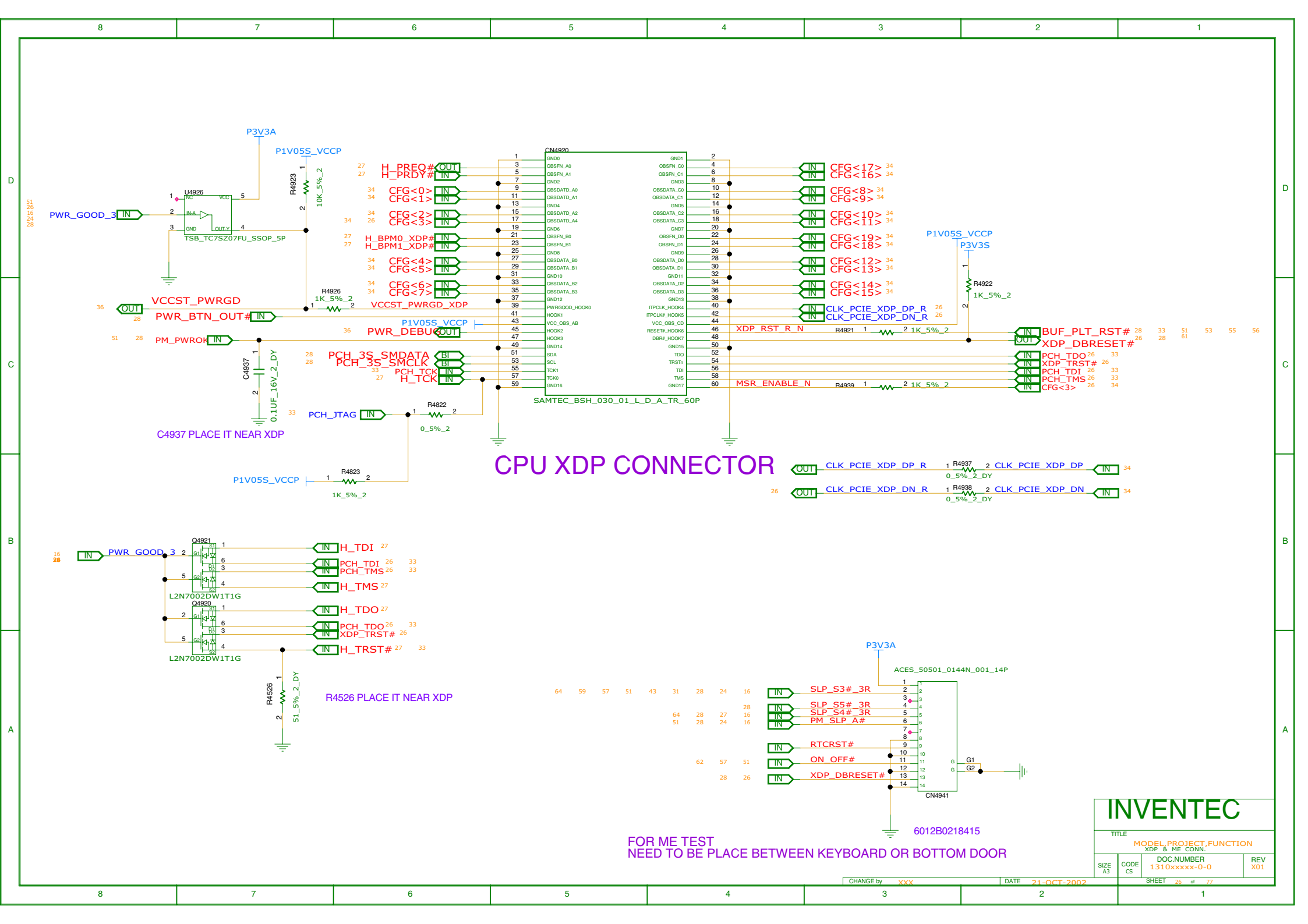
AMBIENT TEMP SENSE  
WILL BE NOT USED IN 2013?



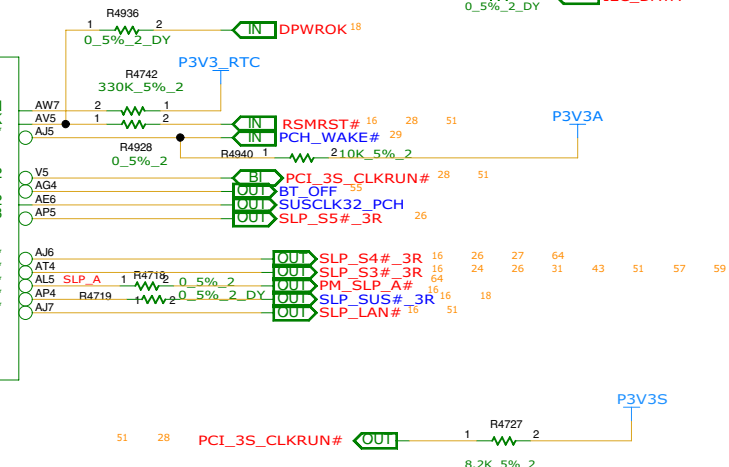
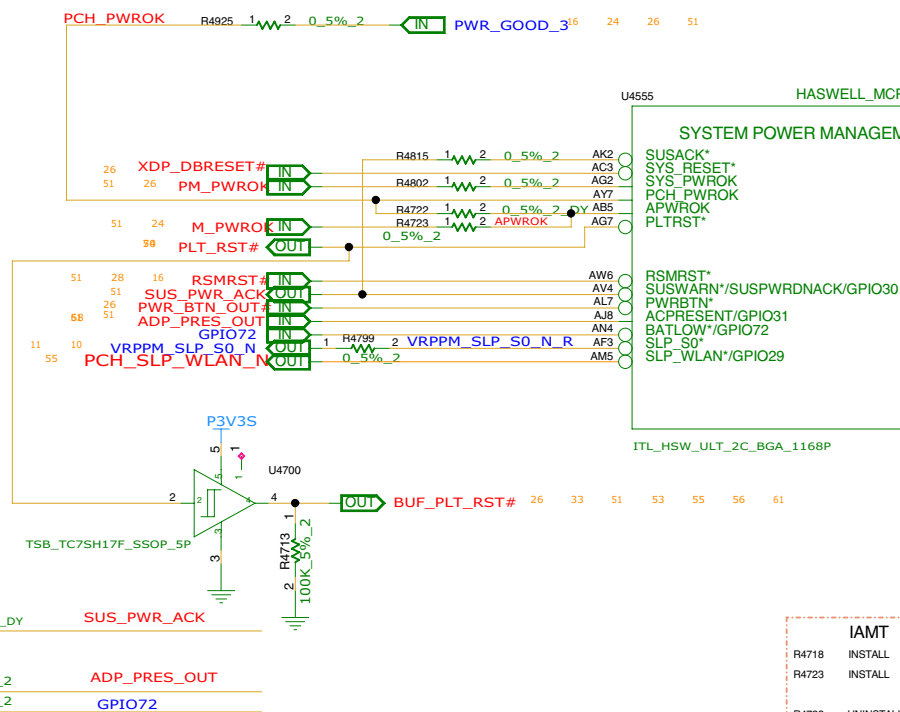
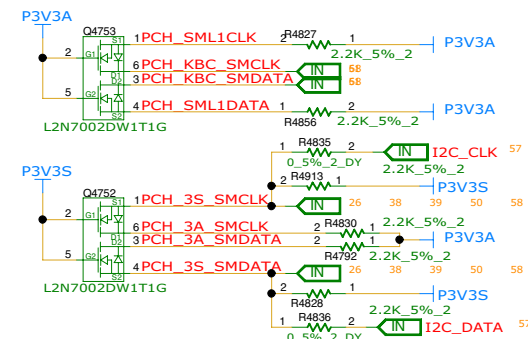
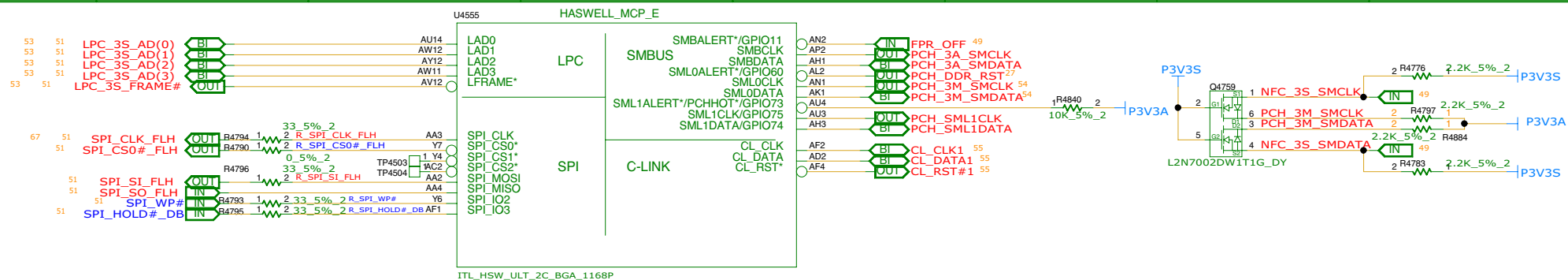
REFERENCE NUMBER:4411~4449

INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
FAN & THERMAL			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 25 of 77			







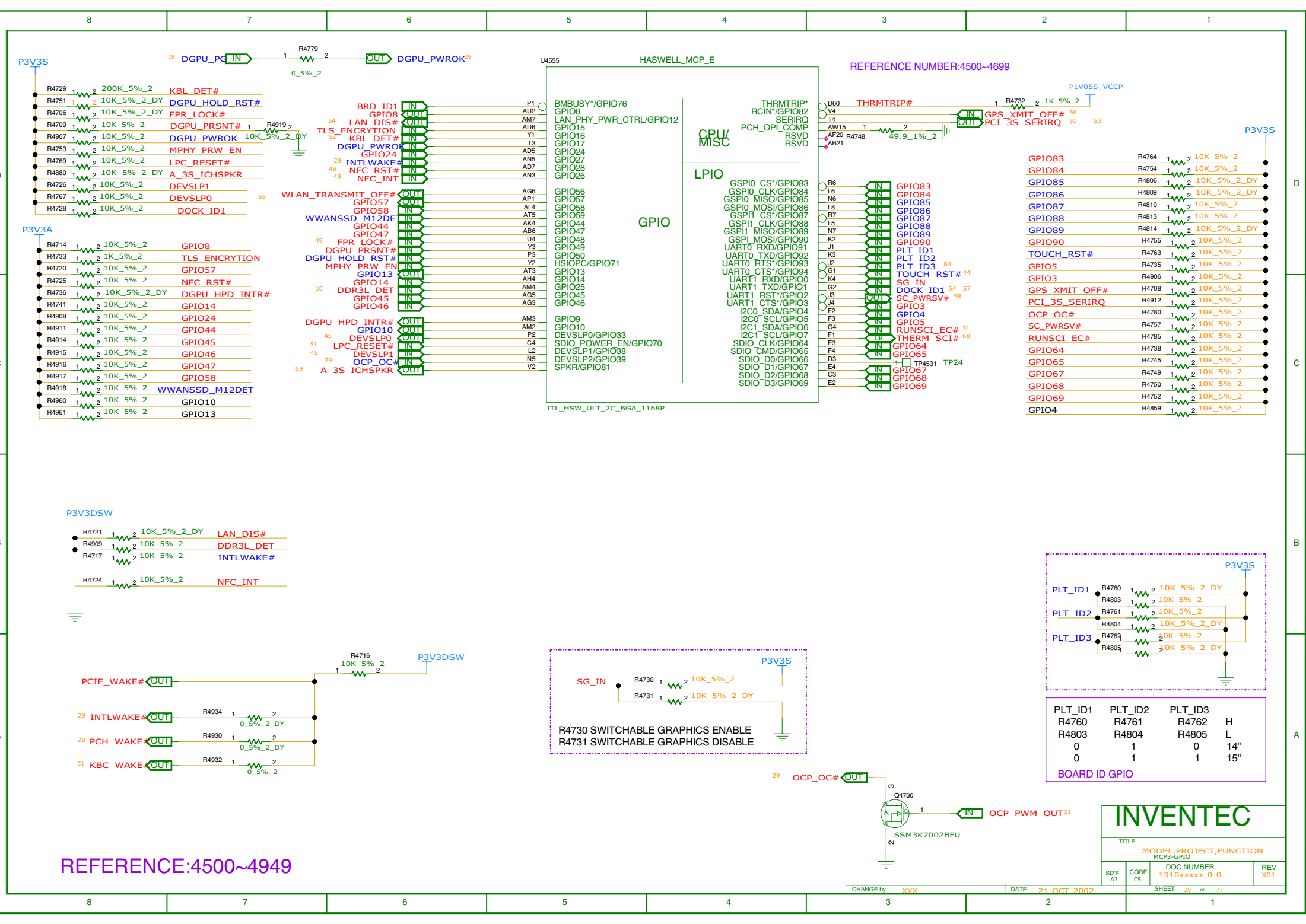
	IAMT	NON-IAMT
R4718	INSTALL	UNINSTALL
R4723	INSTALL	UNINSTALL
R4722	UNINSTALL	INSTALL

REFERENCE:4500~4949

# INVENTEC

TITLE				MODEL,PROJECT,FUNCTION	
MCP2-SPI,SMBUS,SYSTEM				SRQENCE	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0		RE X0	
SHEET 28 of 77					

CHANGE by	XXX	DATE	21-OCT-2002
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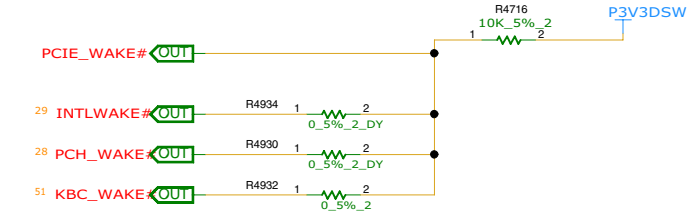
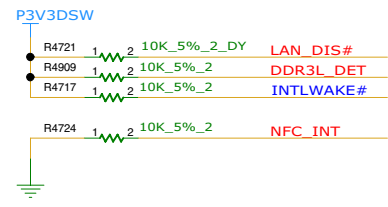
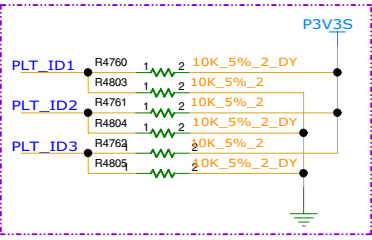
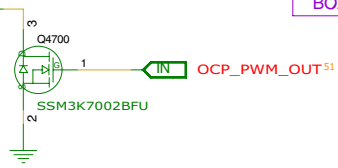
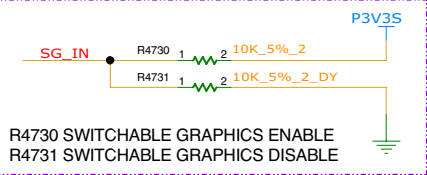


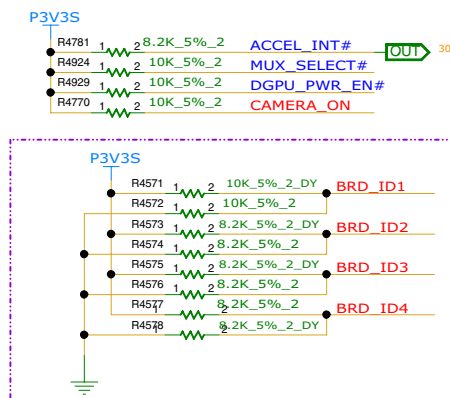
REFERENCE:4500~4949

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
MCP3-GPIO			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

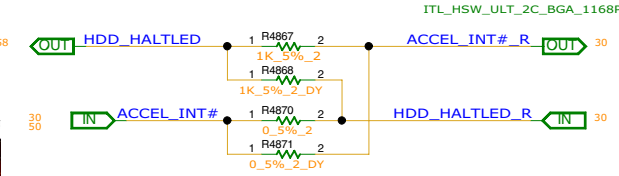
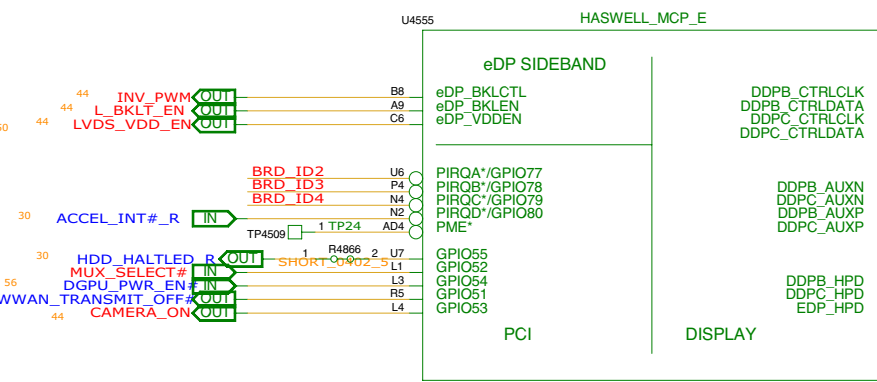
PLT_ID1	PLT_ID2	PLT_ID3	
R4760	R4761	R4762	H
R4803	R4804	R4805	L
0	1	0	14"
0	1	1	15"

BOARD ID GPIO



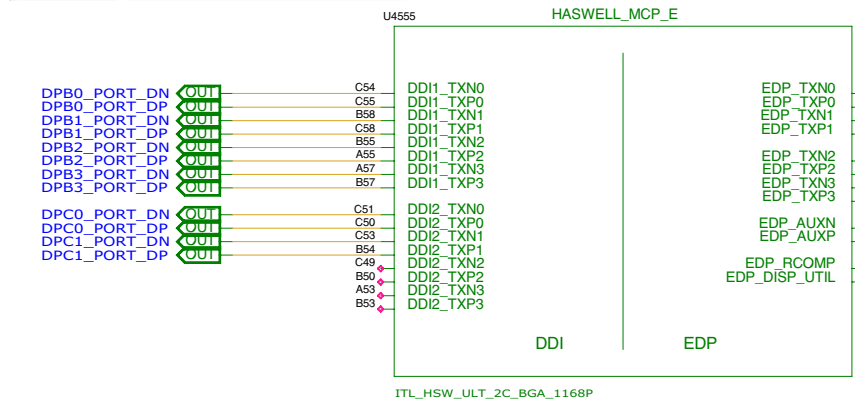
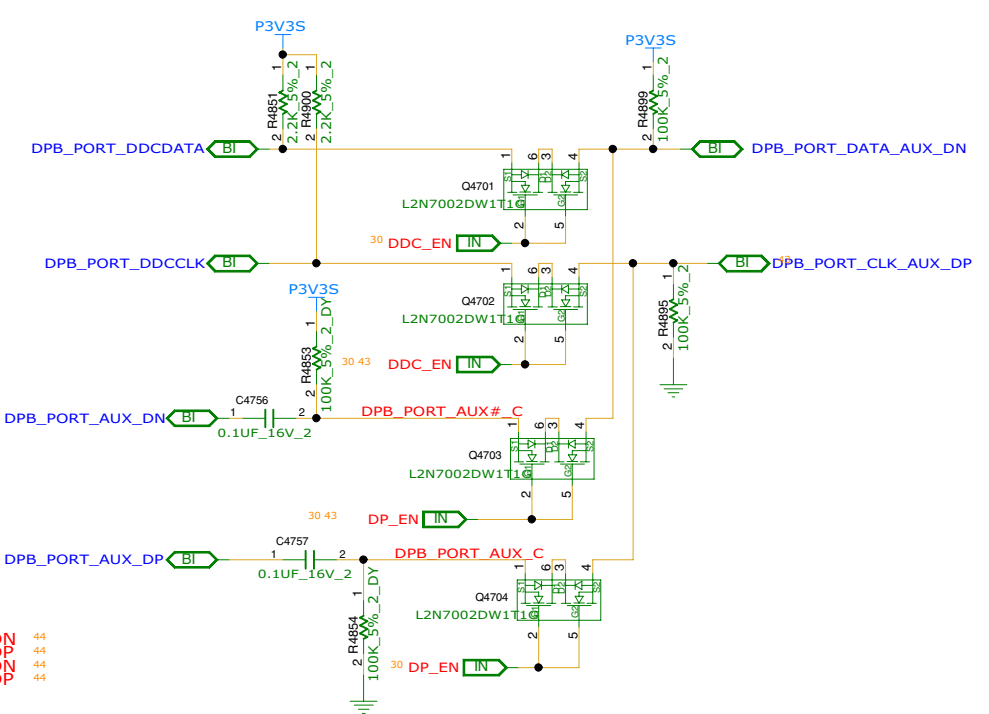


	BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
	GPIO201	GPIO202	GPIO203	GPIO204	AMD_FCH
	GPIO14	GPIO34	GPIO35	GPIO40	FPNT
	GPIO15	GPIO34	GPIO35	GPIO40	LPT-H
BOARD REVISION	GPIO76	GPIO77	GPIO78	GPIO79	LPT-LP
DB 0	0	0	0	0	0
DB 1	0	0	0	0	1
DB 2	0	0	1	0	0
SI 1	0	0	1	1	1
SI 1B	0	1	0	1	0
SI 2	0	1	1	0	0
	0	1	1	1	1
PV 1	1	0	0	0	0
	1	0	0	1	1
	1	0	1	0	0
	1	0	1	1	1
MV	1	1	0	0	0
	1	1	0	1	1
	1	1	1	0	0
	1	1	1	1	1



BRD_ID1	BRD_ID2	BRD_ID3	BRD_ID4	
R4571	R4573	R4575	R4577	H
R4572	R4574	R4576	R4578	L
0	0	0	0	DB0
0	0	0	1	DB1

COMMON PLATFORMS SYSTEM BOARD ID GPIO



REFERENCE:4500~4949

INVENTEC

TITLE

MODEL PROJECT, FUNCTION

DOC NUMBER

1310xxxxx-0-0

REV

X01

SIZE

A3

CODE

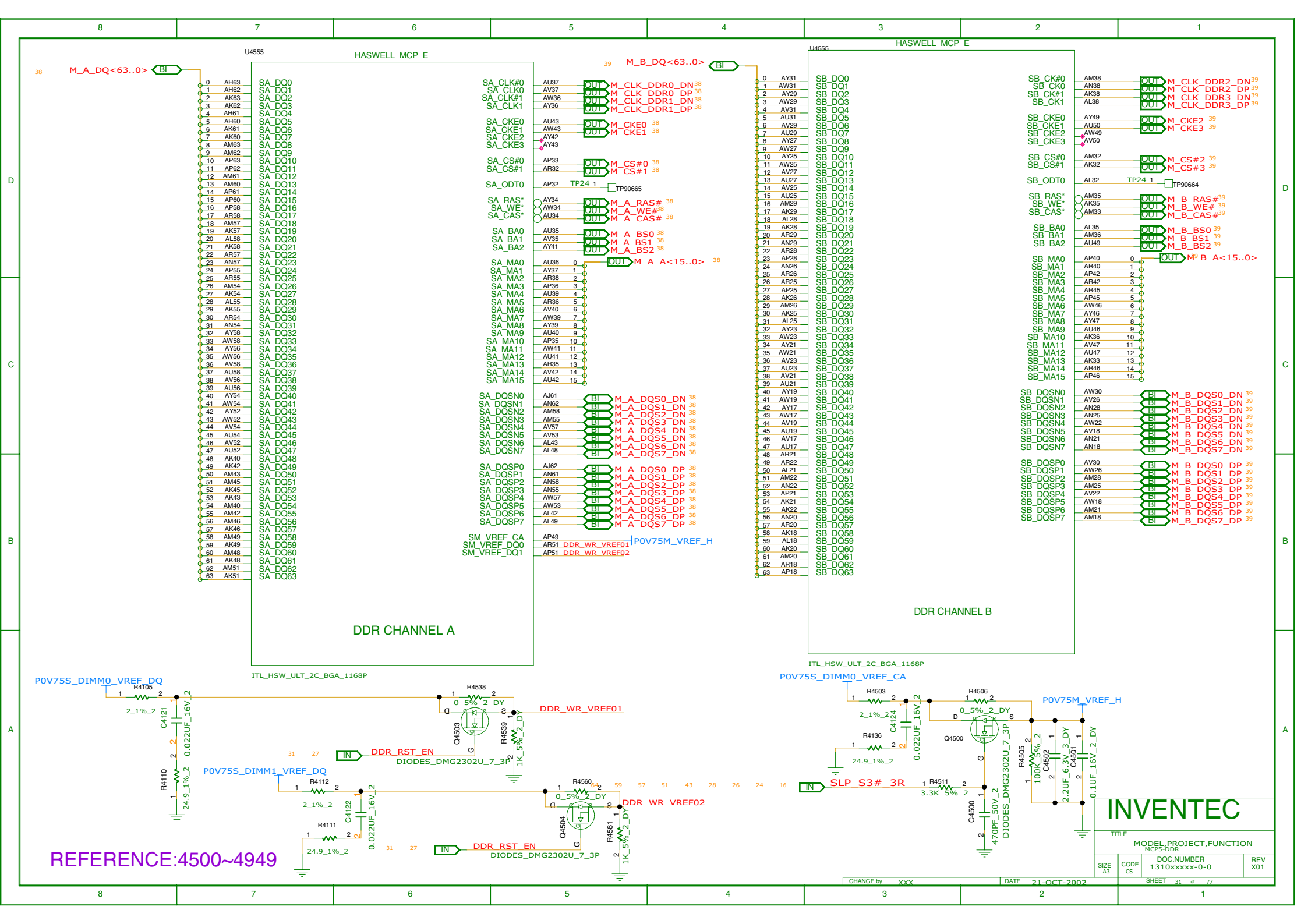
CS

SHEET

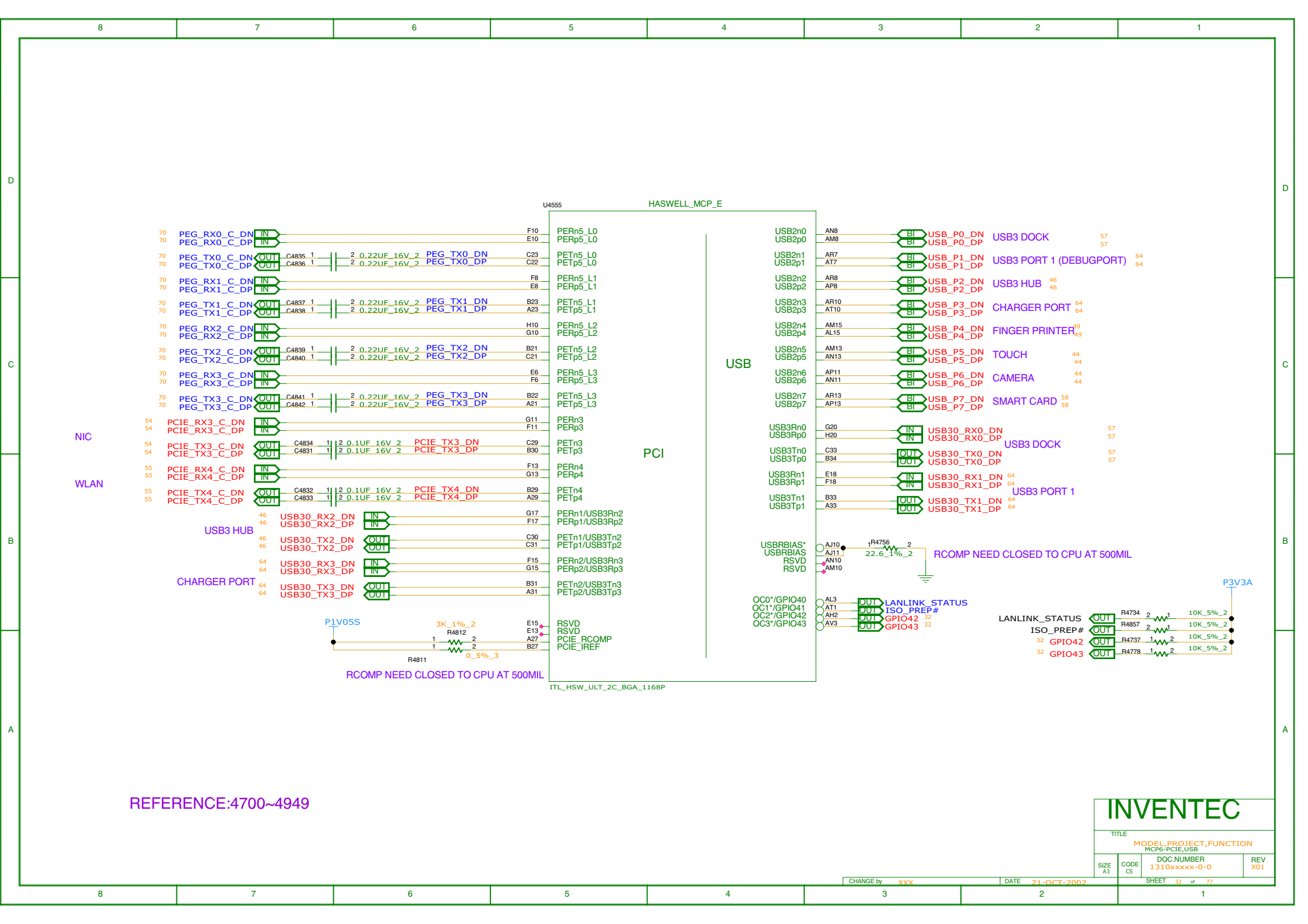
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of

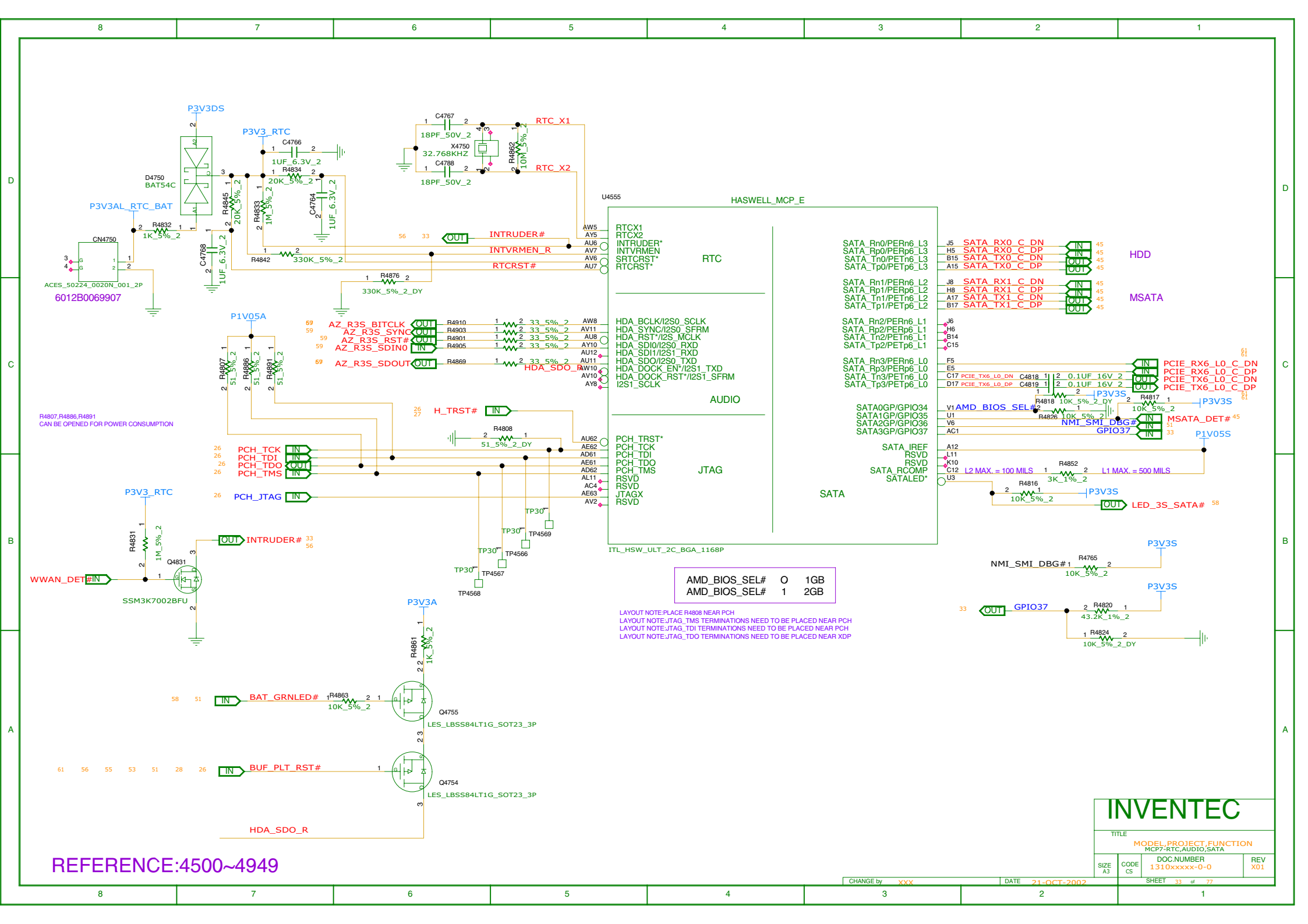
77







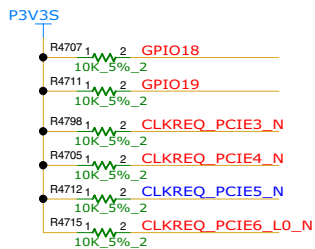




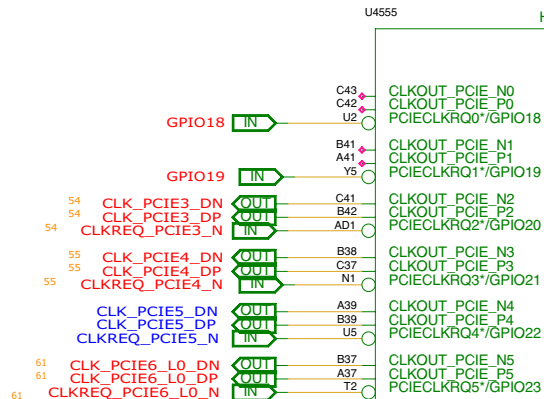
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INVENTEC

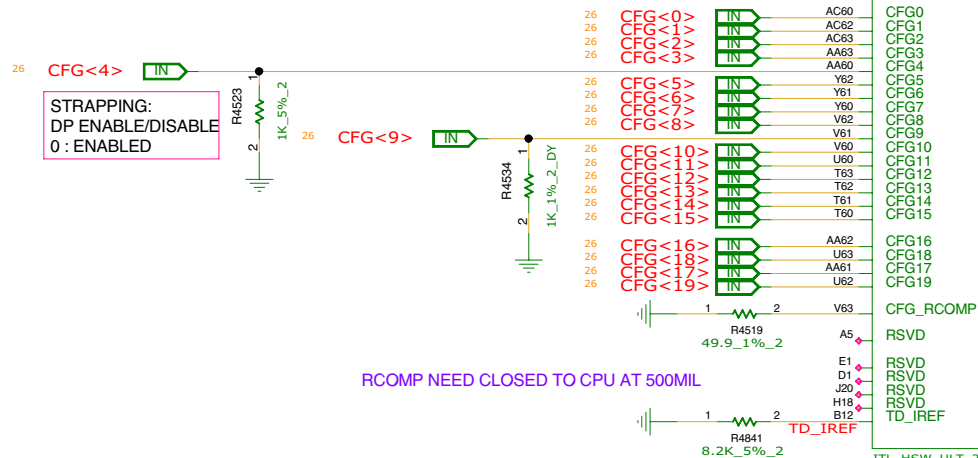
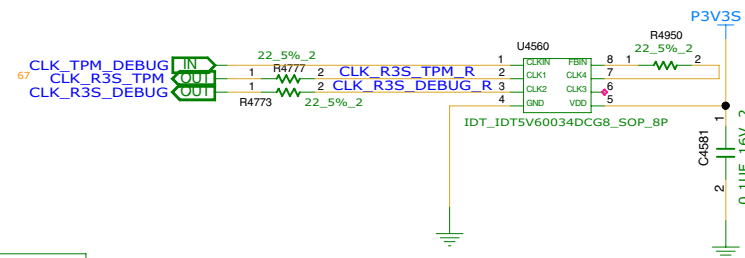
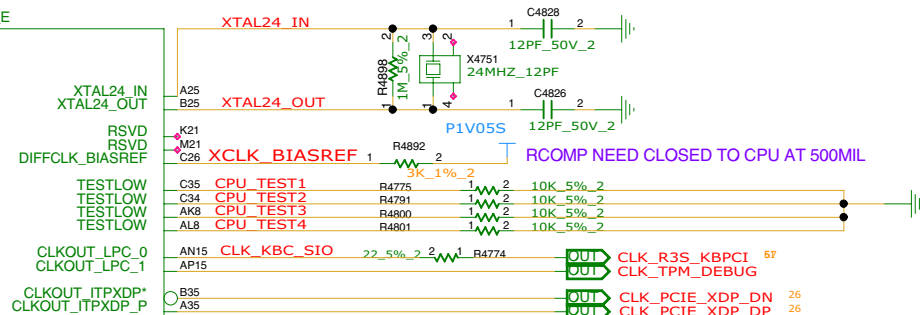
TITLE			
MODEL PROJECT FUNCTION			
MCP7-RTC,AUDIO,SATA			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01



NIC  
WLAN  
MARS  
SD/MMC



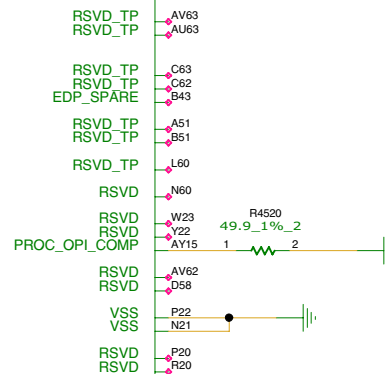
ITL\_HSW\_UL\_T2C\_BGA\_1168P



RCOMP NEED CLOSED TO CPU AT 500MIL

RESERVED

ITL\_HSW\_UL\_T2C\_BGA\_1168P



REFERENCE:4500~4949

INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
MCP8-CLOCK,RESERVED

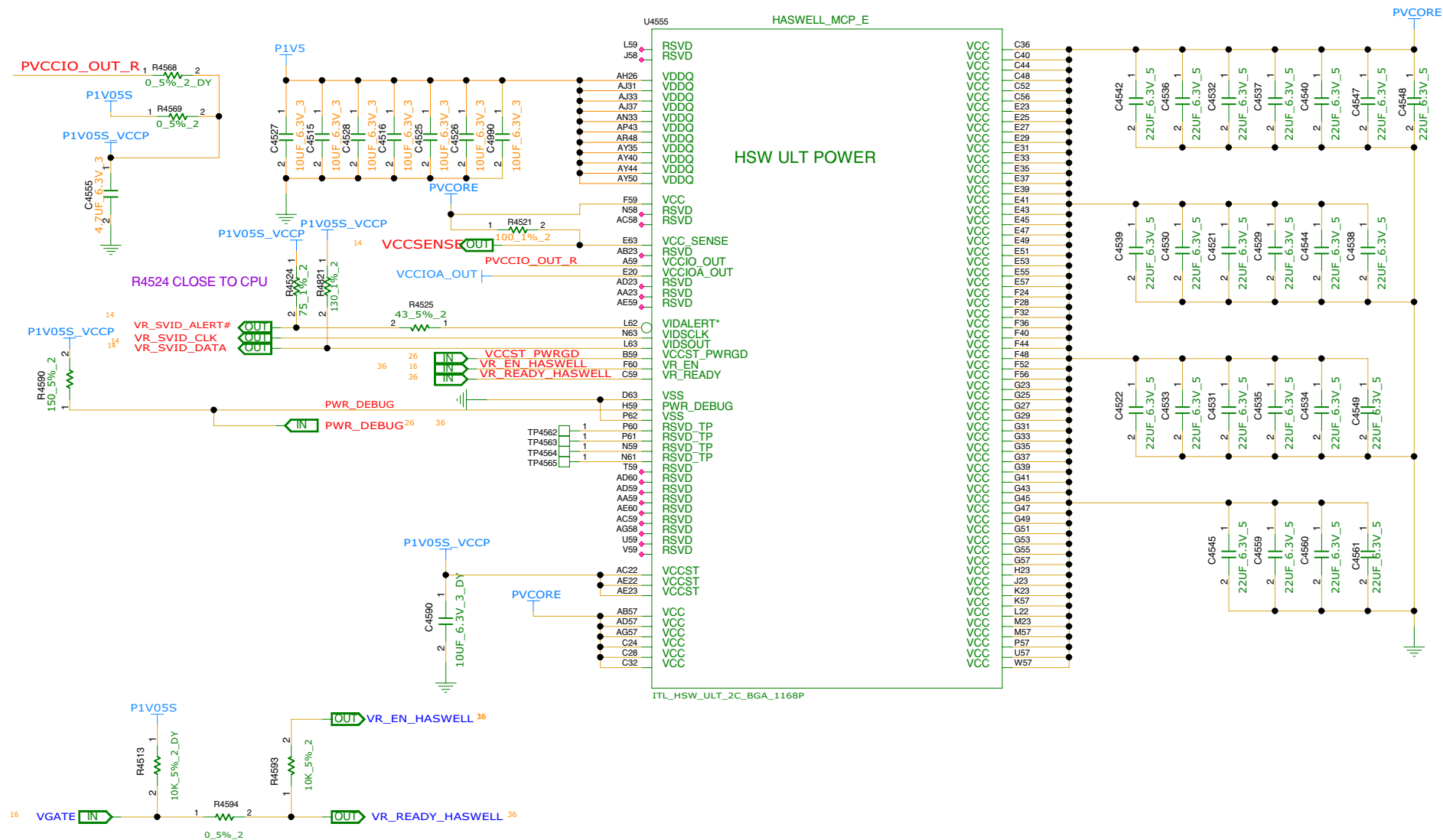
SIZE CODE DOC NUMBER REV  
A3 CS 1310XXXXX-0-0 X01

CHANGE by XXX DATE 21-OCT-2002

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ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE

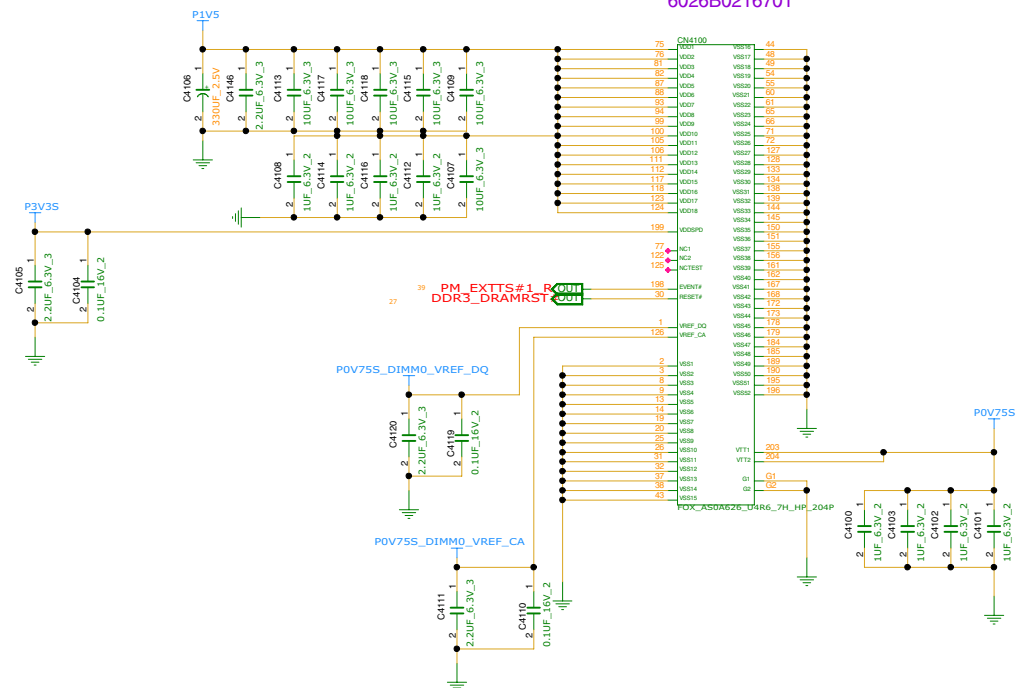
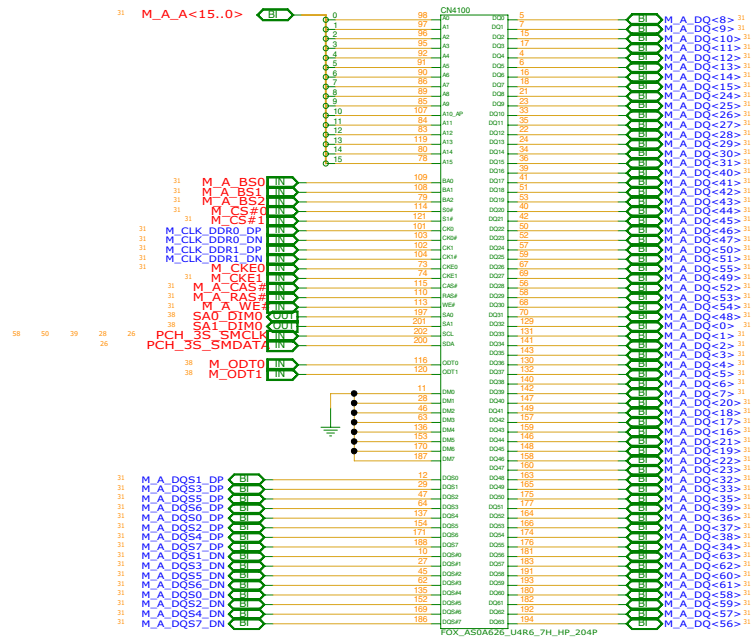


REFERENCE:4500~4949

INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
MCP10-POWER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

100%

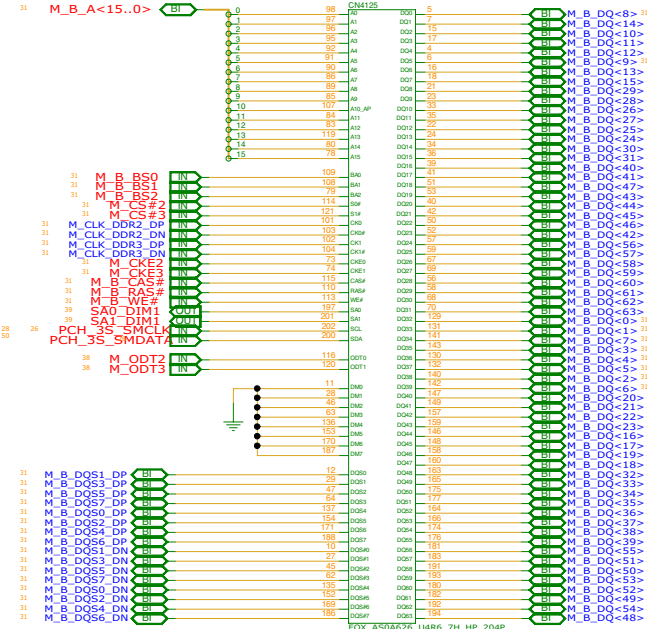
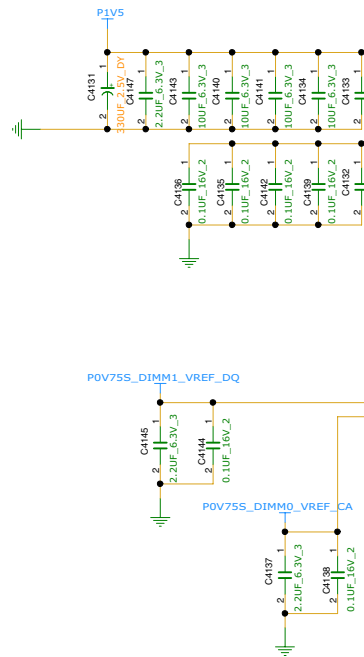
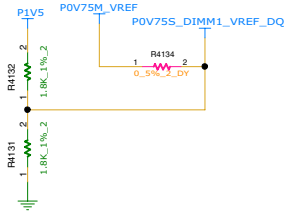


INVENTEC

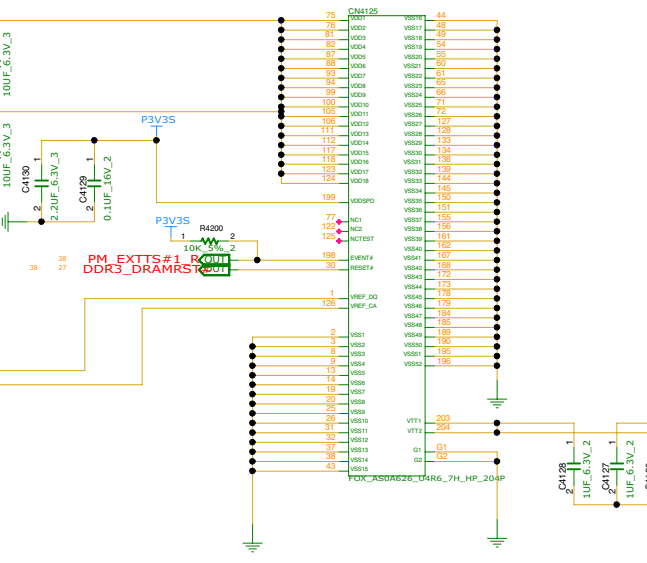
TITLE			
MODEL,PROJECT,FUNCTION DDR3_SO-DIMM0			
SIZE C	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 38 of 77			

NOTE:  
SO-DIMM SPD ADDRESS IS 0X04  
SO-DIMM TS ADDRESS IS 0X34

REFERENCE NUMBER:4100~4299



6026B0216701



INVENTEC			
MODEL,PROJECT,FUNCTION			
DDR3_SO-DIMM0			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310A0000-0-0	201
SHEET		38	of 37

RESERVED

INVENTEC

TITLE			
MODEL PROJECT FUNCTION DPB DEMUX1 TO DP			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 40 of 77			

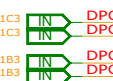


RESERVED

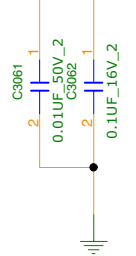
INVENTEC

TITLE			
MODEL PROJECT FUNCTION DPC DEMUX2 TO VGA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 41 of 77			

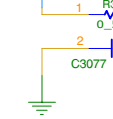
PIN 2	3393 R3062 C3069 C3070	3355 R3061
PIN 5	R3065	R3063 C3077
PIN 8		C3061 C3062
PIN 11	C3073	
PIN 14	R3064 C3074	R3080
PIN 15		R3078
PIN 16		R3067
PIN 17		R3079
PIN 27	L3066 C3087	
PIN 35	C3068	R3081
PIN 36	R3077	
PIN 37	R3074	R3076
PIN 38	10K_DY	R3075 C3090 C3091
PIN 39		L3068 C3092
PIN 40		R3092



P1V5\_VDD



P3V3S\_DVDD33



P3V3S\_DVDD33



42C8 41A1

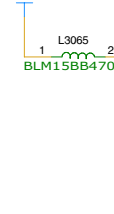


42C8 41A1

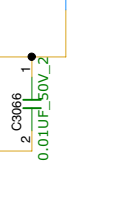


CHECK IF DEMUX NOT NEED R3079,R3080

P3V3S



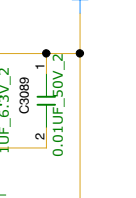
P3V3S\_DVDD33



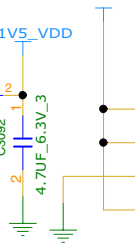
P3V3S\_DVDD33



P3V3S\_AVDD33



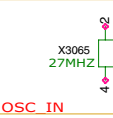
P3V3S\_DVDD33



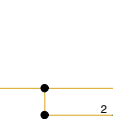
P1V5\_VDD



OSC\_OUT



OSC\_IN



P1V5\_VDD



CRT\_R



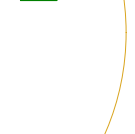
OUT CRT\_R\_L



CRT\_G



OUT CRT\_G\_L



CRT\_B

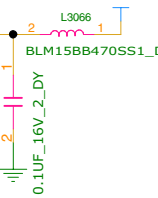


OUT CRT\_B\_L



FOR EMI

P3V3S\_DVDD33



CRT\_R

CRT\_G

CRT\_B

CRT\_HSYNC

CRT\_VSYNC

CRT\_DDCDATA

CRT\_DDCCLK

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

CRT\_VSYNC

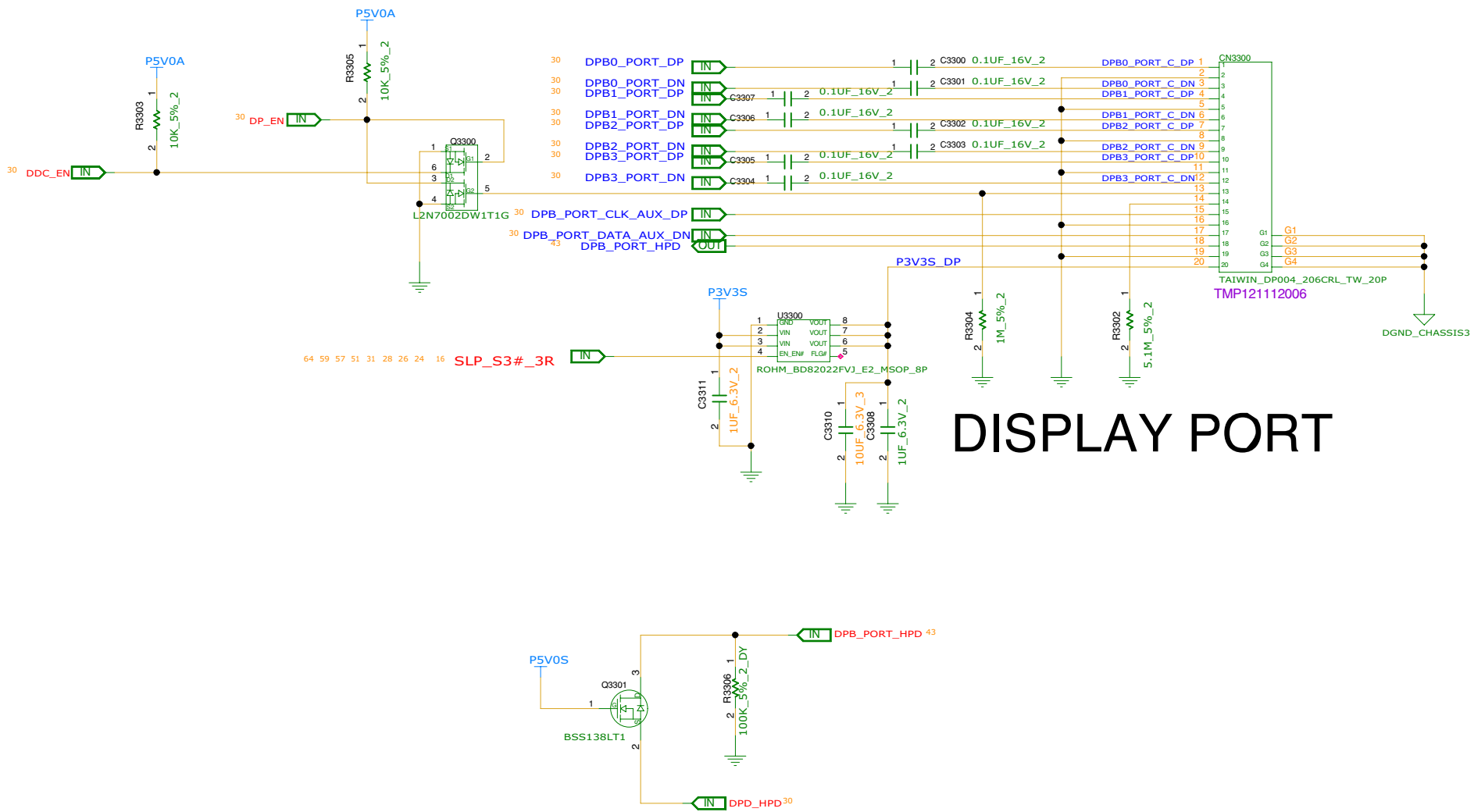
CRT\_HSYNC

CRT\_VSYNC

CRT\_HSYNC

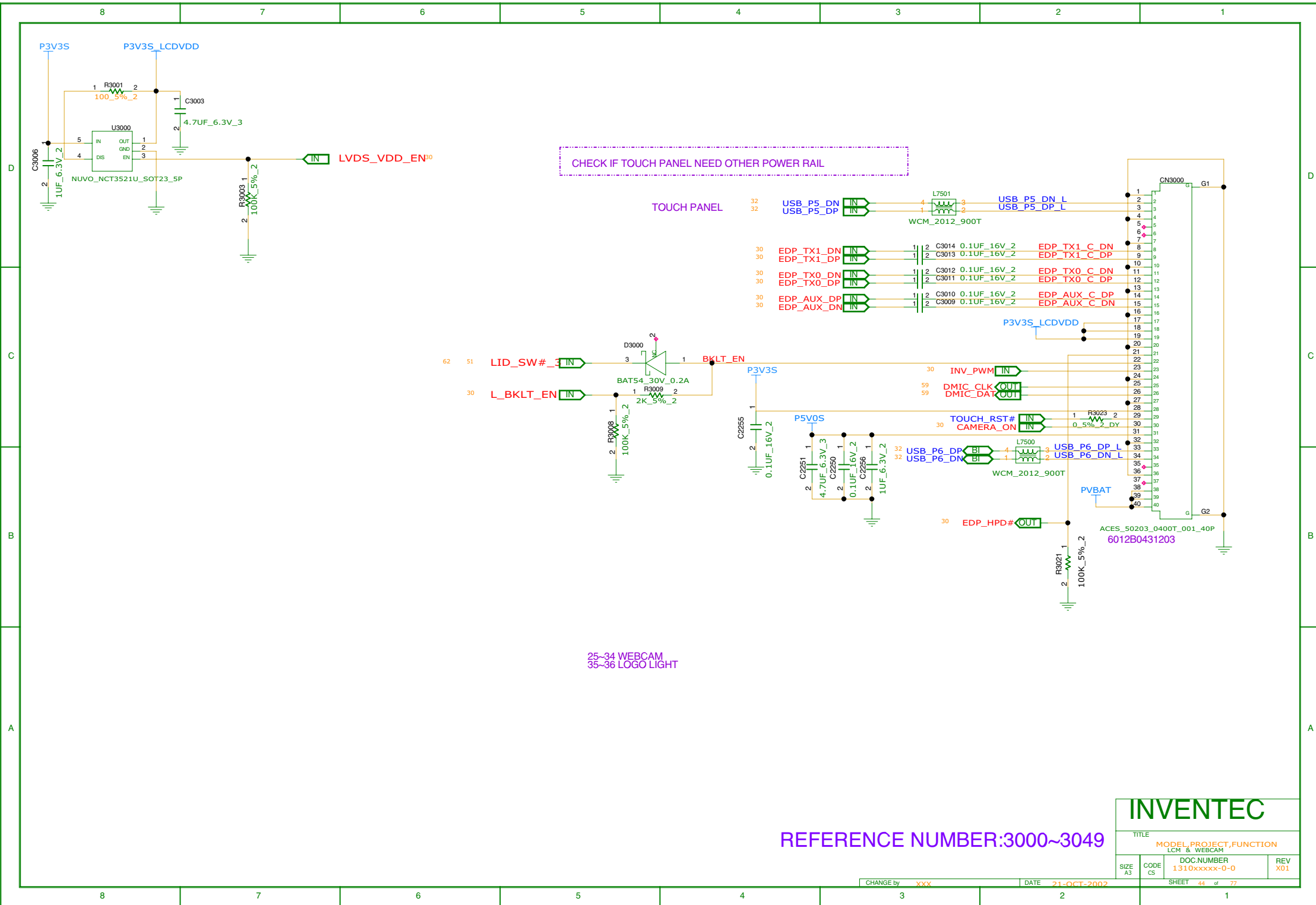
CRT\_VSYNC

INVENTEC			
TITLE			
MODEL PROJECT/FUNCTION			
DP-TO-VGA CONVERTER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	42 of 77



REFERENCE NUMBER:3300~3399

INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
CRT & DP			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 43 of 77			



REFERENCE NUMBER:1700~1749

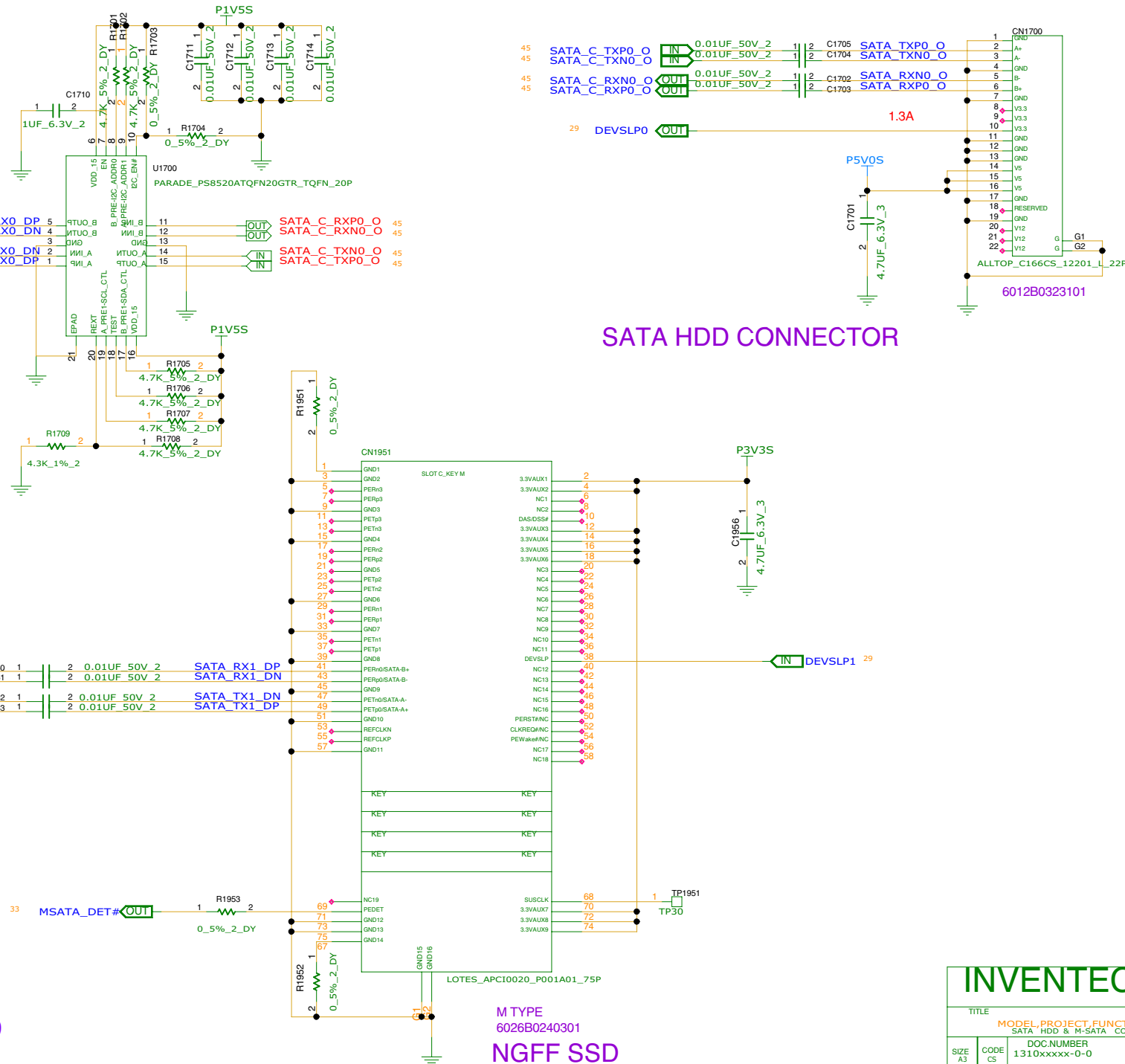
REFERENCE NUMBER:1950~1999

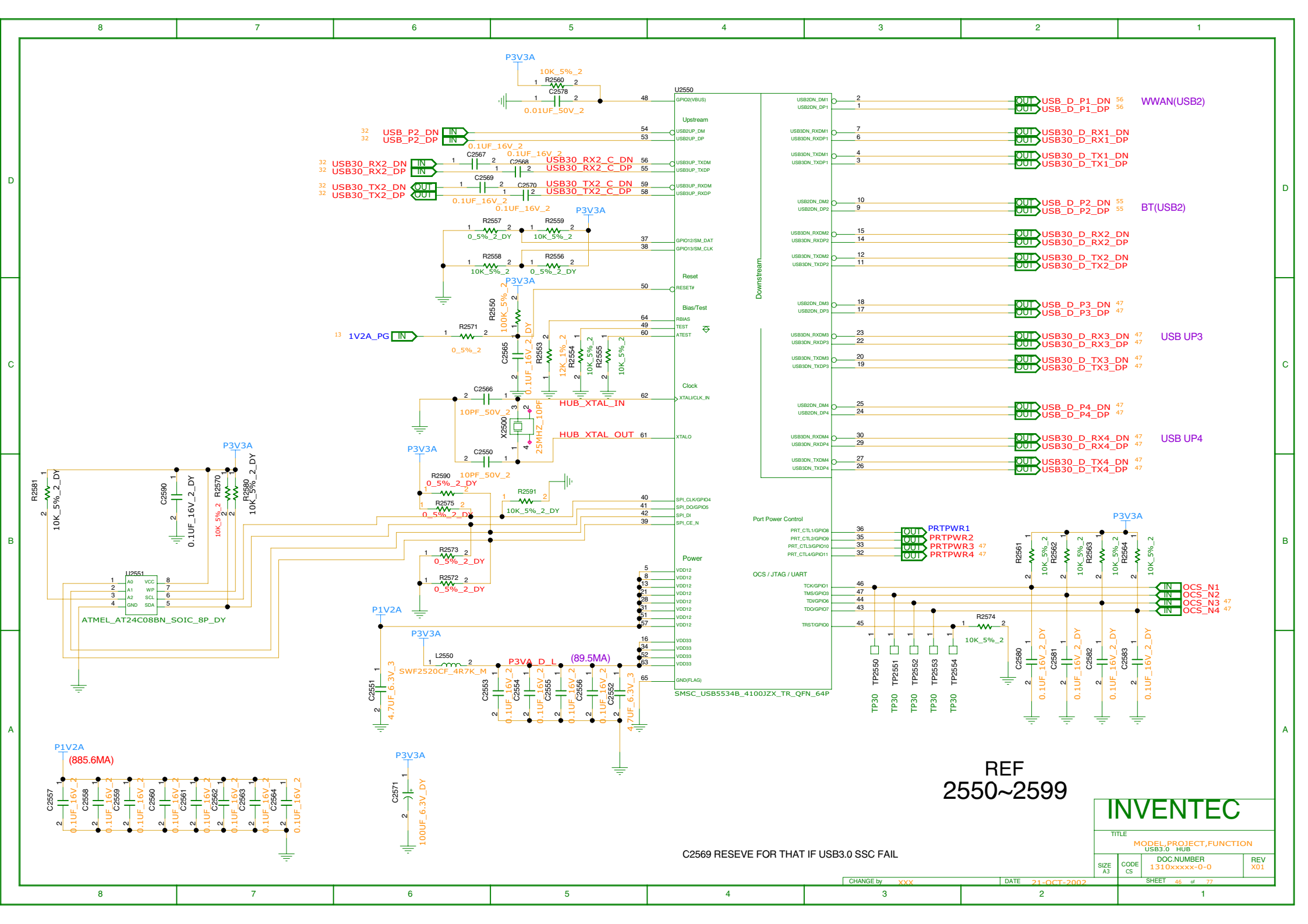
M TYPE  
6026B0240301  
NGFF SSD

SATA HDD CONNECTOR

INVENTEC

TITLE			
MODEL,PROJECT,FUNCTION			
SATA, HDD & M-SATA CONN.			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 45 of 77			

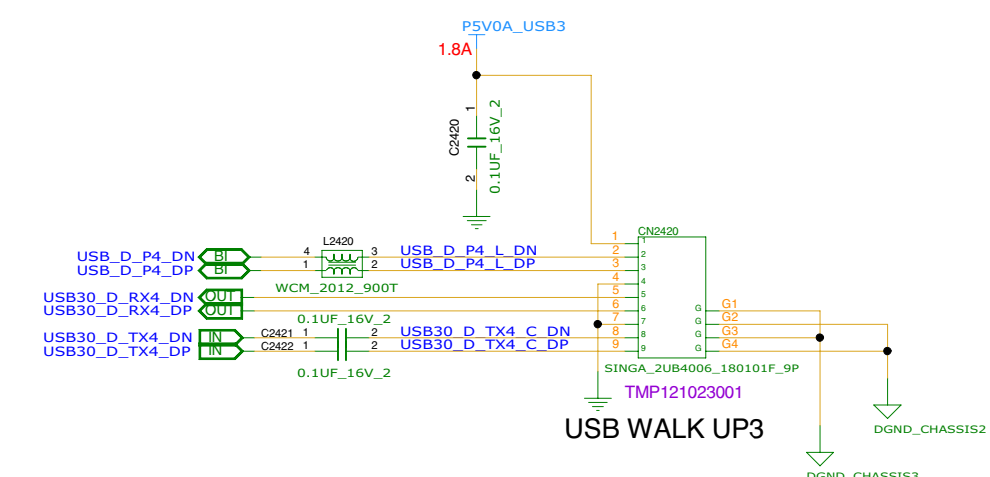
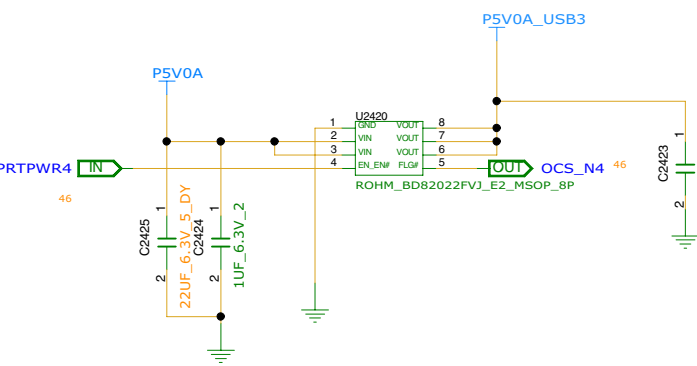
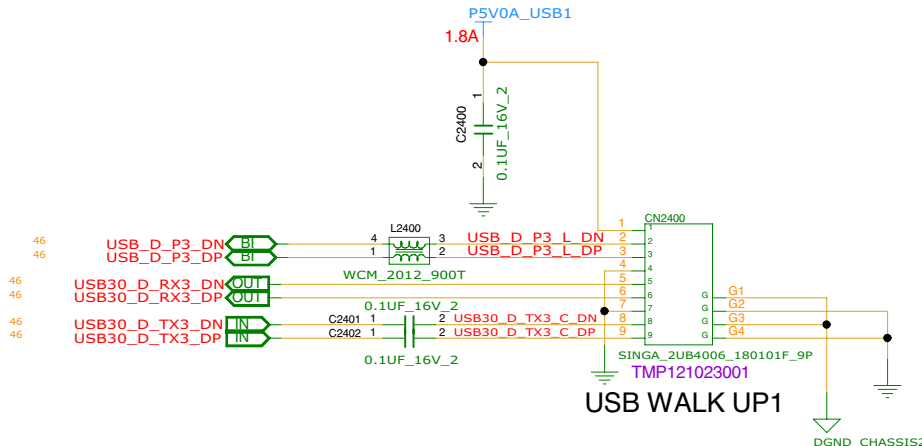
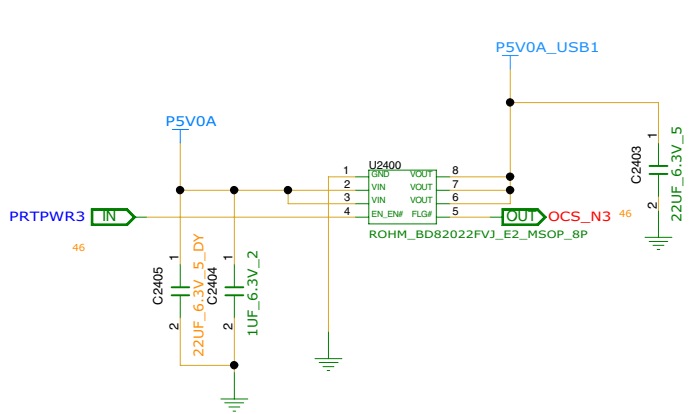




C2569 RESEVE FOR THAT IF USB3.0 SSC FAIL

REF  
2550~2599

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
USB3.0 HUB			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

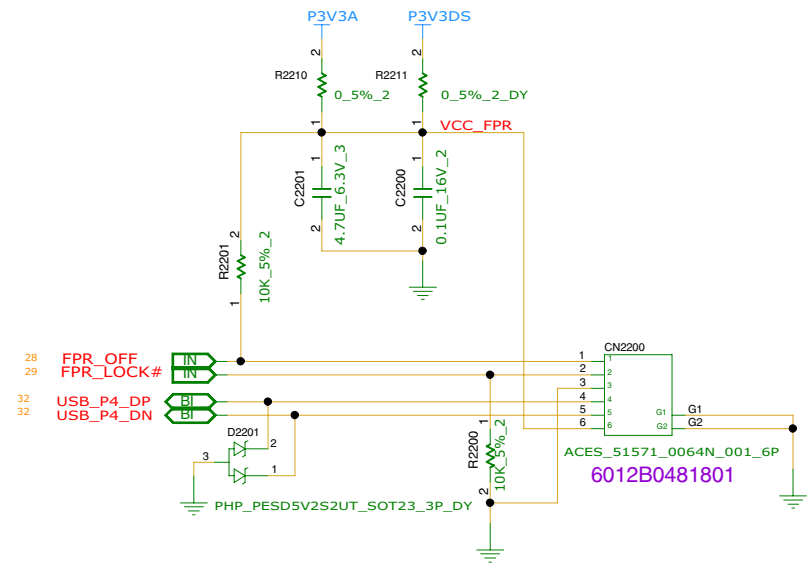


REFERENCE NUMBER:2400~2499

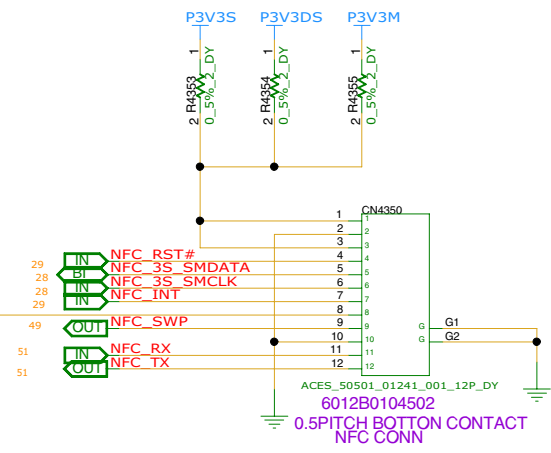
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
USB & USB CHARGER			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
CHANGE by XXXX			
DATE 21-OCT-2002			
SHEET 47 of 77			



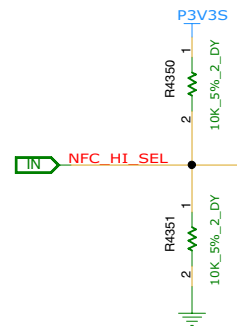




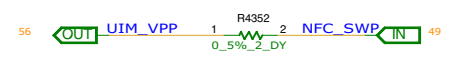
FINGER PRINT CONN



0.5PITCH BOTTOM CONTACT  
NFC CONN



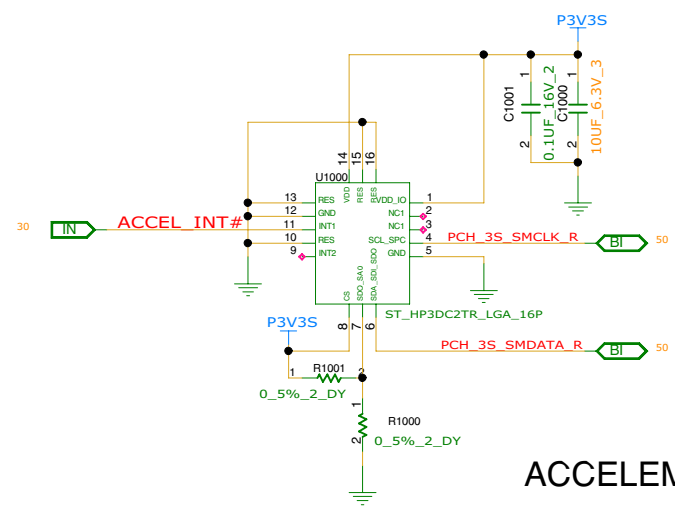
NFC\_HI\_SEL R4350 R4351  
HIGH (UART) INSTALL  
LOW (I2C) INSTALL



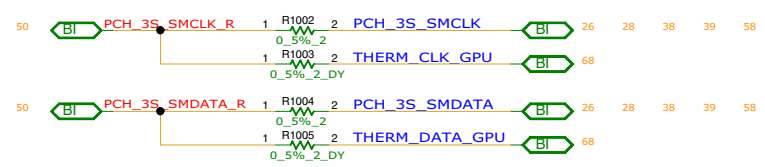
REFERENCE:2200~2249

REFERENCE:4350~4399

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION FINGER PRINTER & NFC			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 49 of 77			

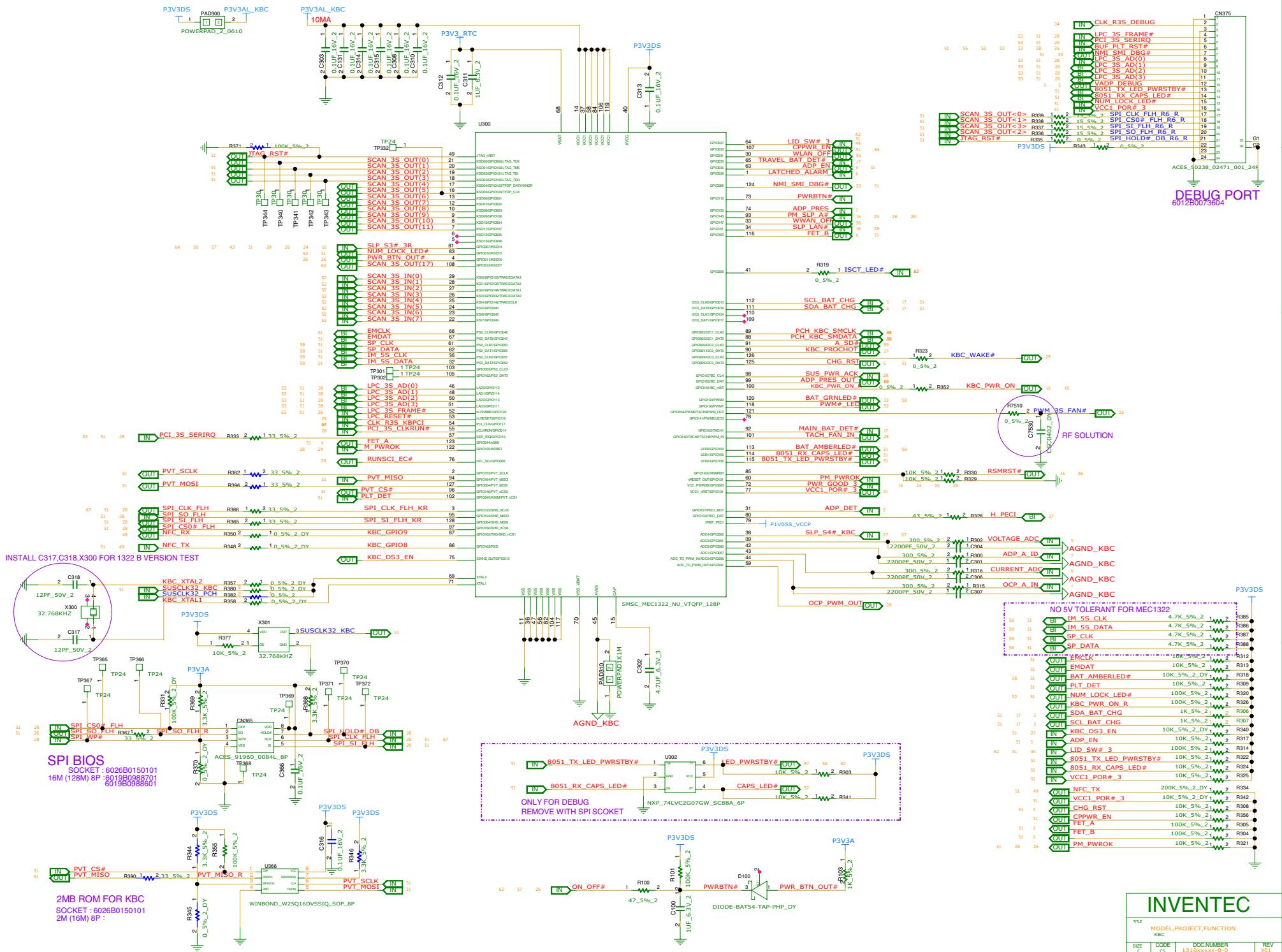


ACCELEMETOR

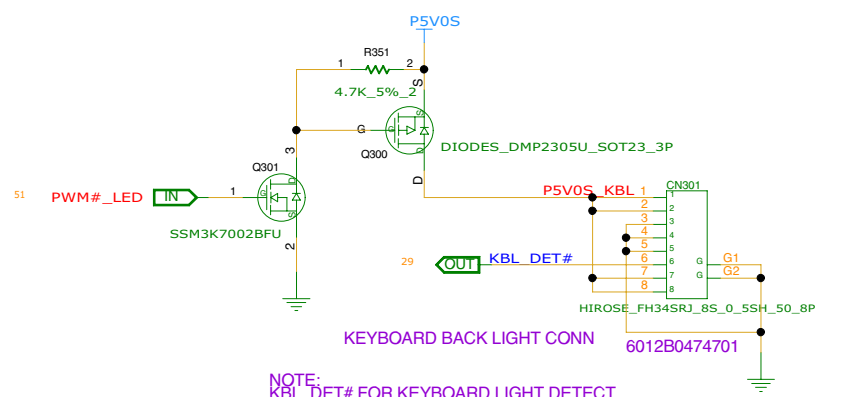
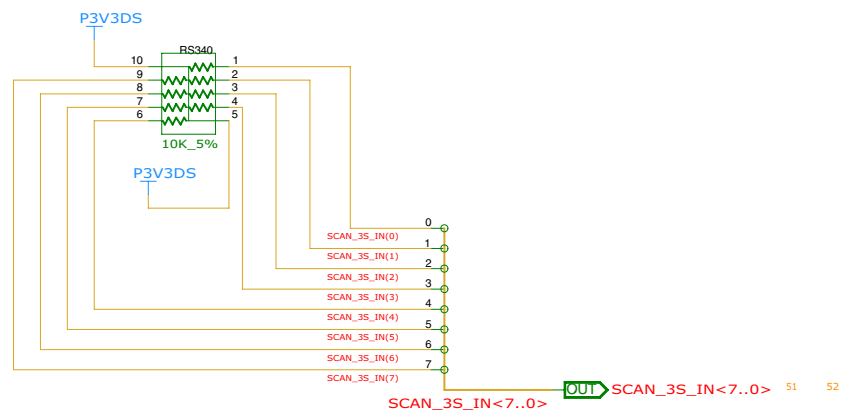
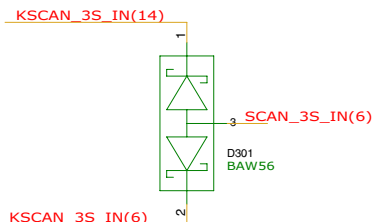
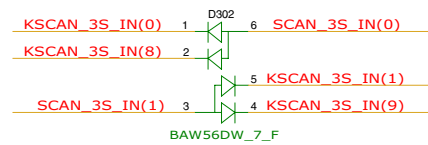
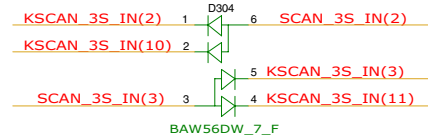
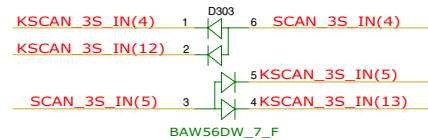
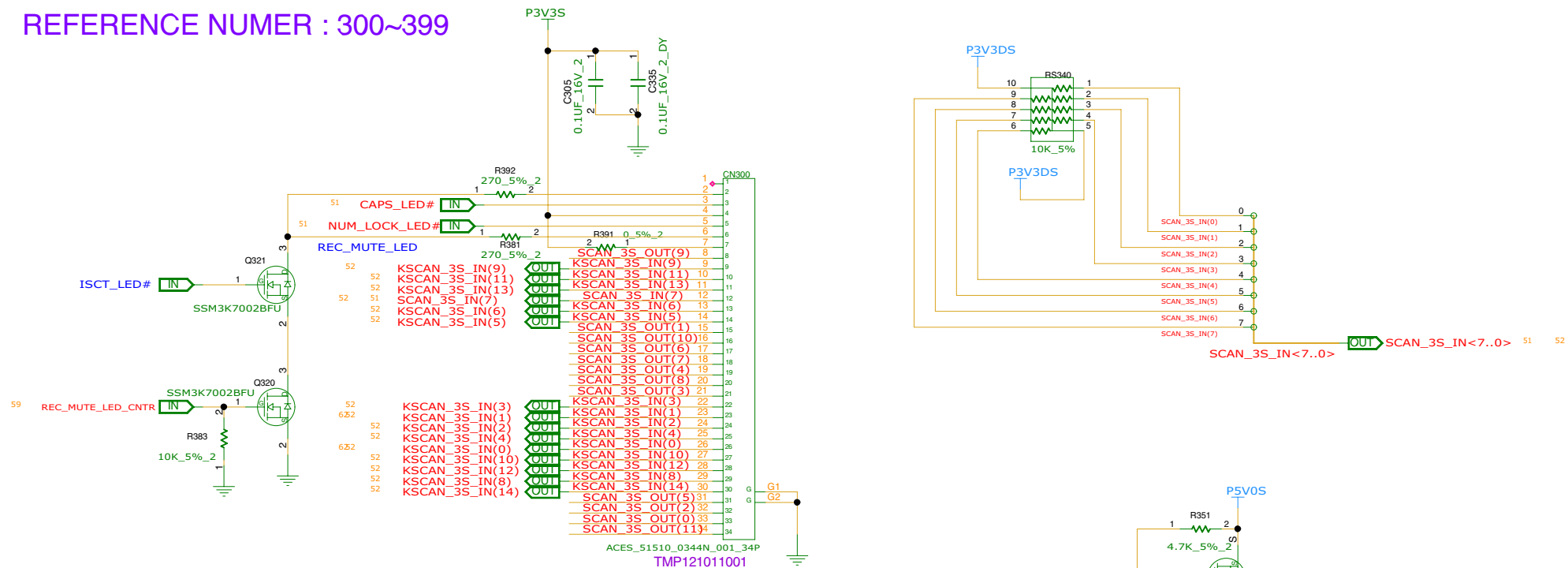


REFERENCE NUMER : 1000~1099

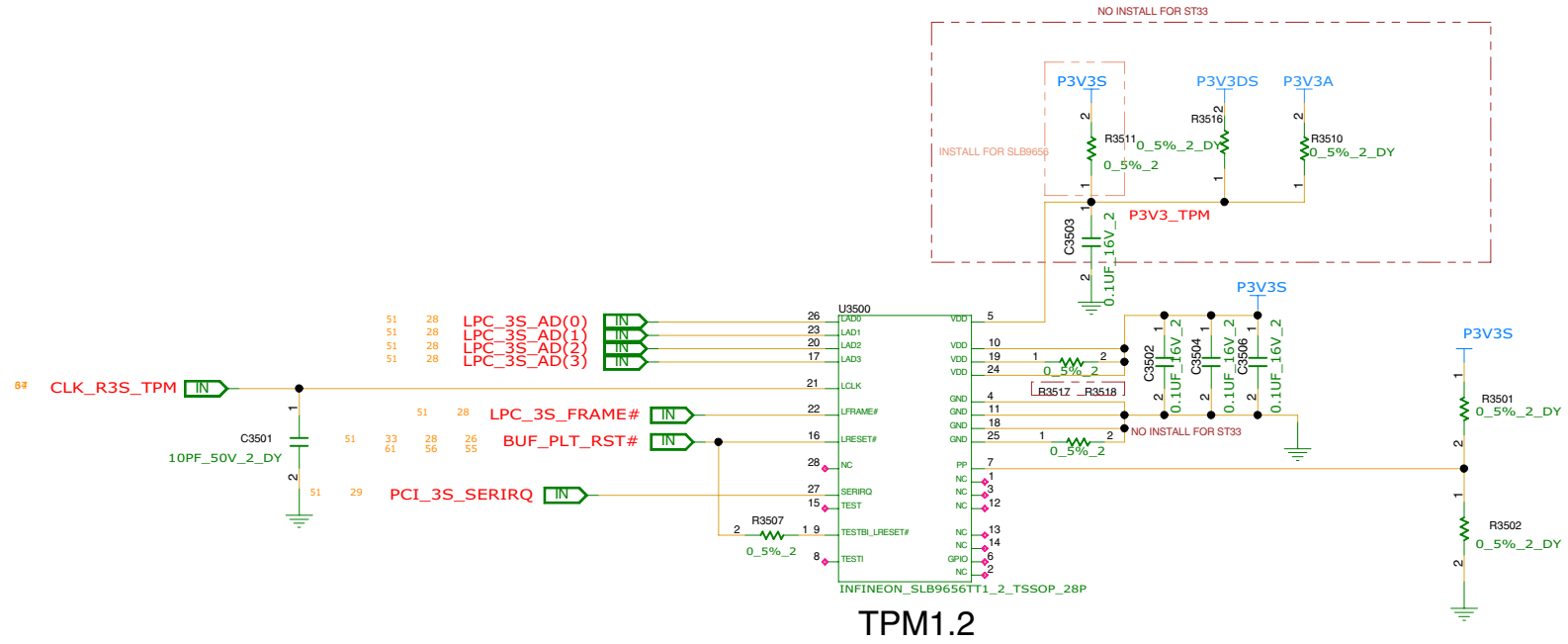
INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION ACCELEMETOR			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 50 of 77			



REFERENCE NUMBER : 300~399



INVENTEC			
TITLE			
MODEL PROJECT,FUNCTION			
KEYBOARD			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 52 of 77			



TPM1.2

SLB9656TT1.2		ST33
C3503	INSTALL	OPEN
R3507	INSTALL	OPEN
R3511	INSTALL	OPEN
R3517	INSTALL	OPEN
R3518	INSTALL	OPEN

REFERENCE NUMER : 3500~3549

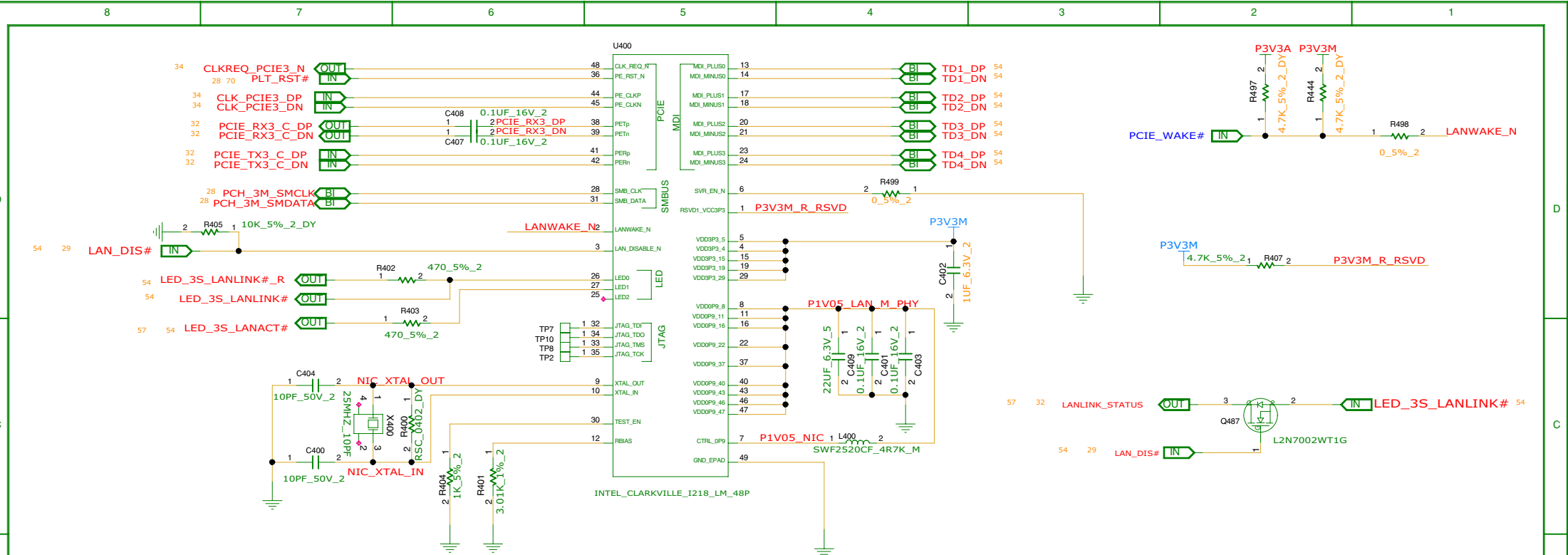
INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
TPM

SIZE CODE DOC NUMBER REV  
A3 CS 1310xxxxx-0-0 X01

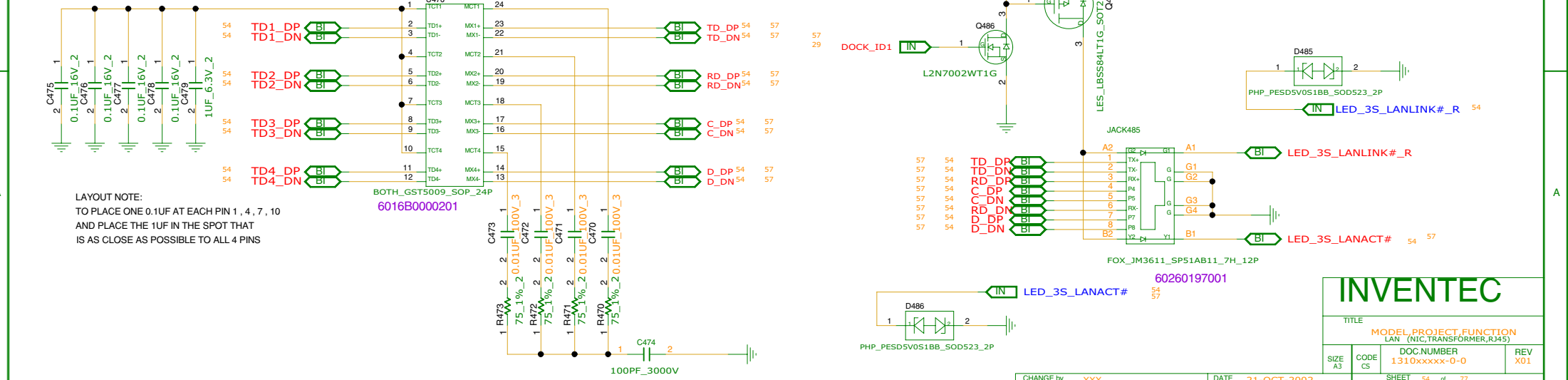
CHANGE by XXX DATE 21-OCT-2002

SHEET 53 of 77



REFERENCE NUMER : 400~469

REFERENCE NUMER : 470~499



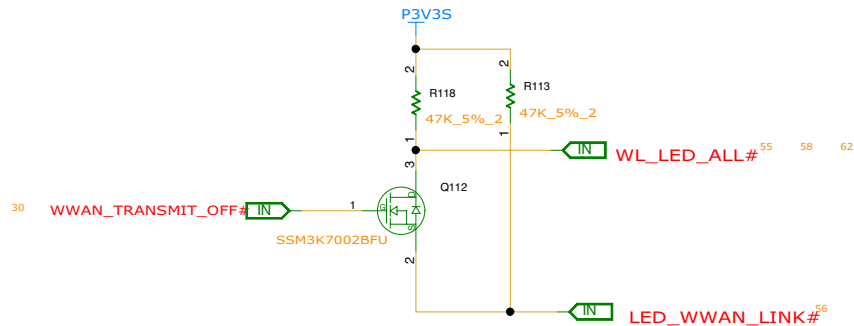
INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
LAN (NIC TRANSFORMER, RJ45)			
DOC NUMBER			
1310xxxx-0-0			
REV			
X01			
SIZE	CODE	DATE	SHEET
A3	CS	21-OCT-2002	54 of 77



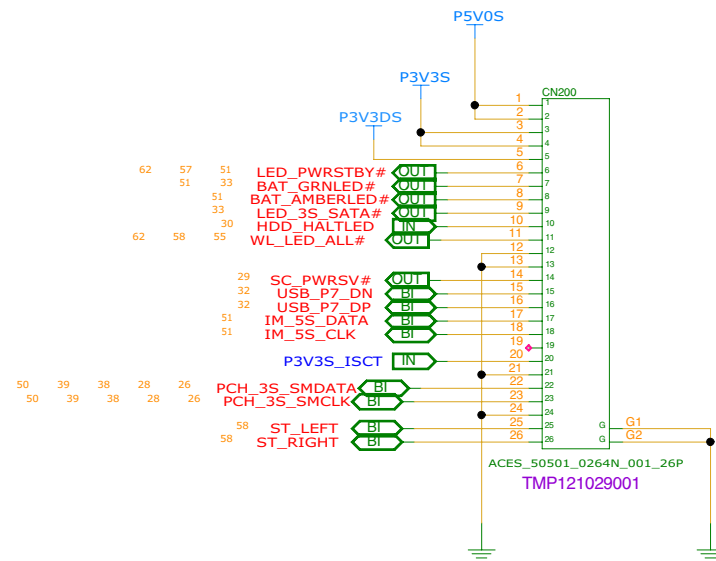




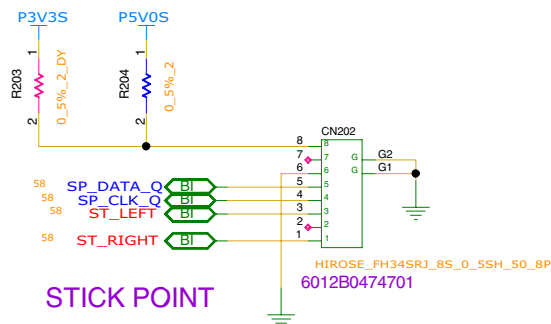




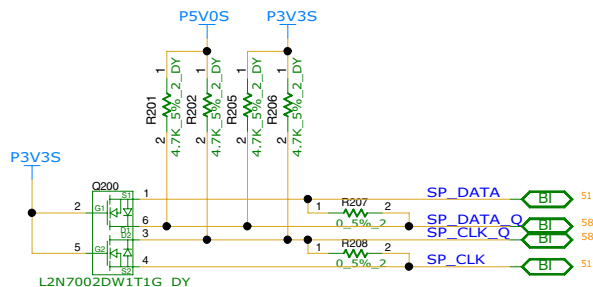
WLAN\_WWAN\_BLUETOOTH\_LED



SMART CARD AND TOUCHPAD D/B W TO B CONN



STICK POINT



STICK POINT OPTION

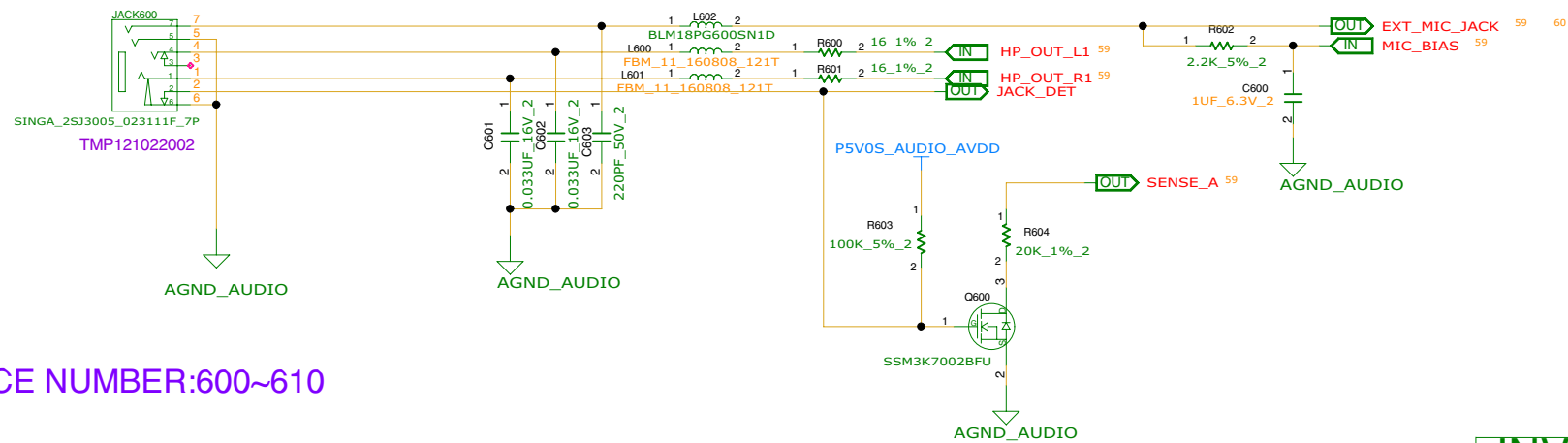
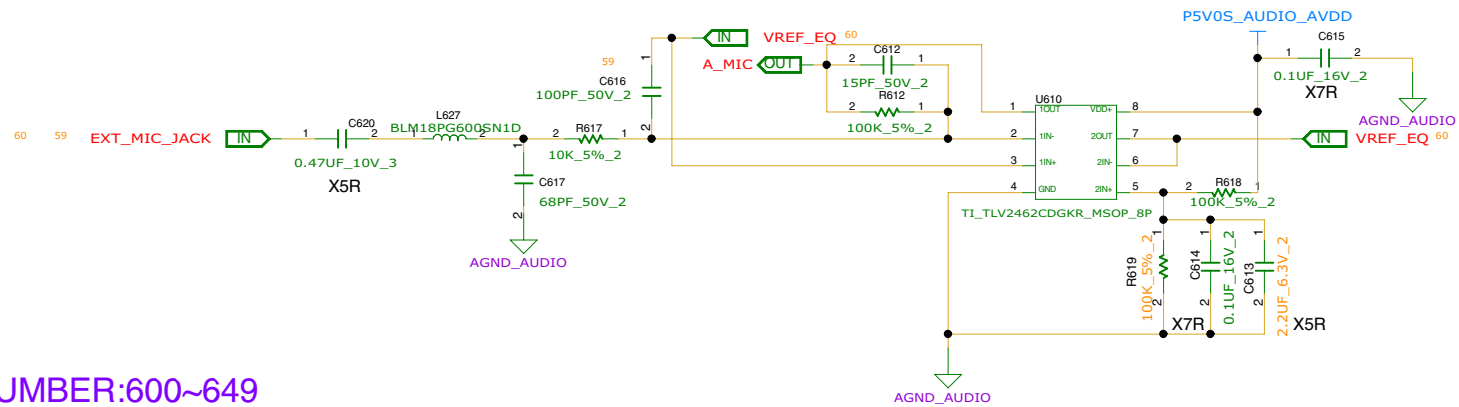
5V	3.3V
R201	INSTALL UNINSTALL
R202	INSTALL UNINSTALL
R203	UNINSTALL INSTALL
R204	INSTALL UNINSTALL

REFERENCE NUMBER:100~199

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
STICK POINT & B2B CNTR			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET 58 of 77			



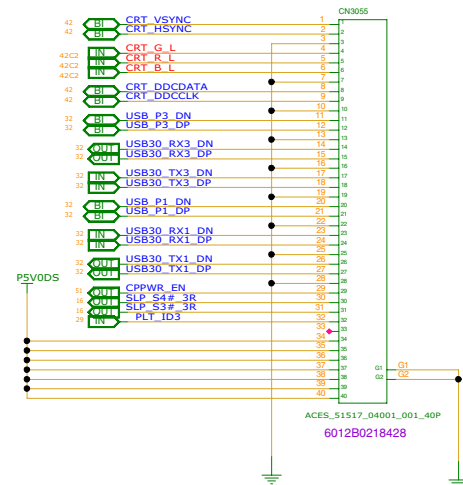
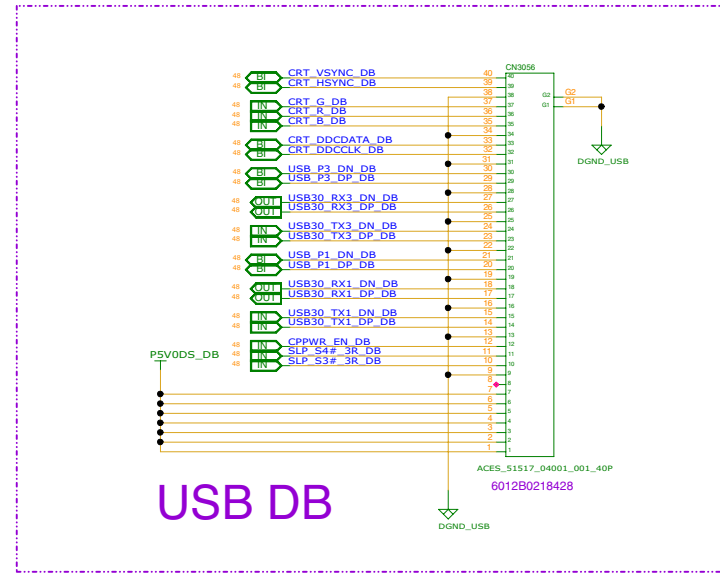


INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
EXT. MIC AMP. & AUDIO JACK			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 60 of 77			











D

D

C

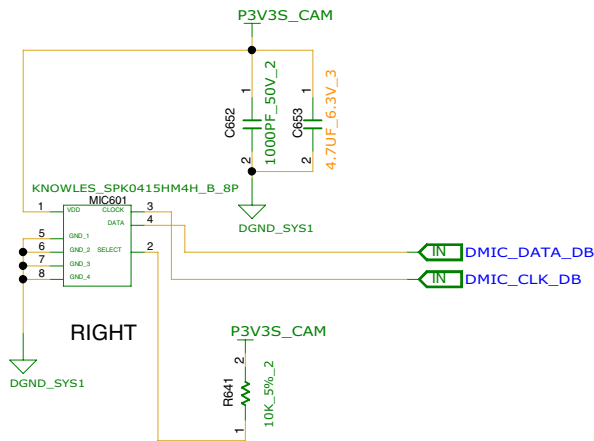
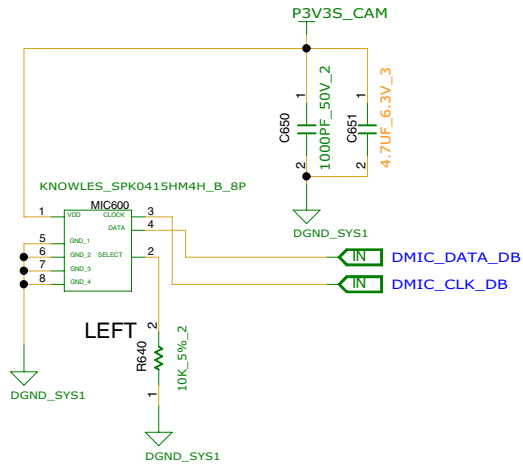
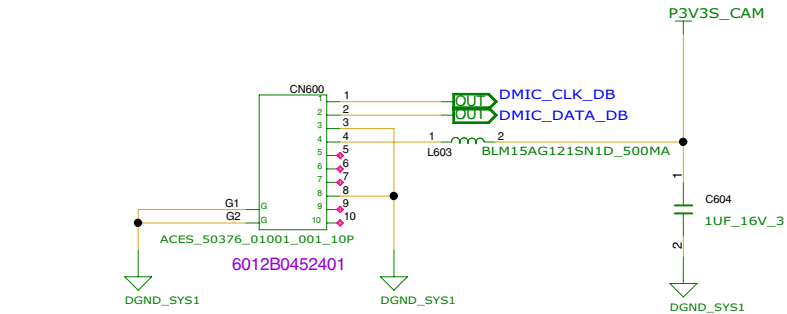
C

B

B

A

A

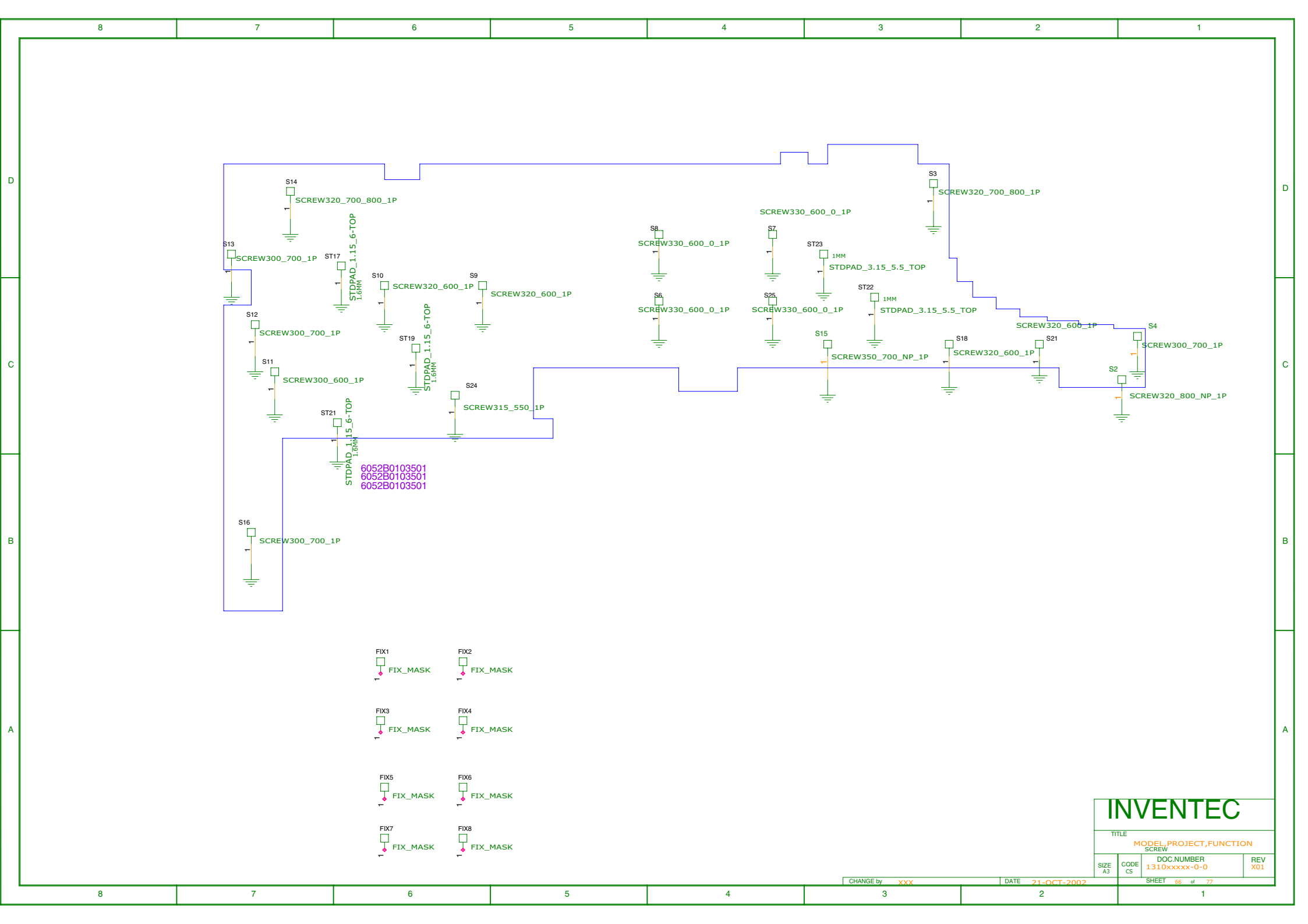


FIX600  
FIX\_MASK

FIX601  
FIX\_MASK

REFERENCE NUMBER:600-649  
MIC DOUGHTER BOARD

INVENTEC			
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 65 of 77			



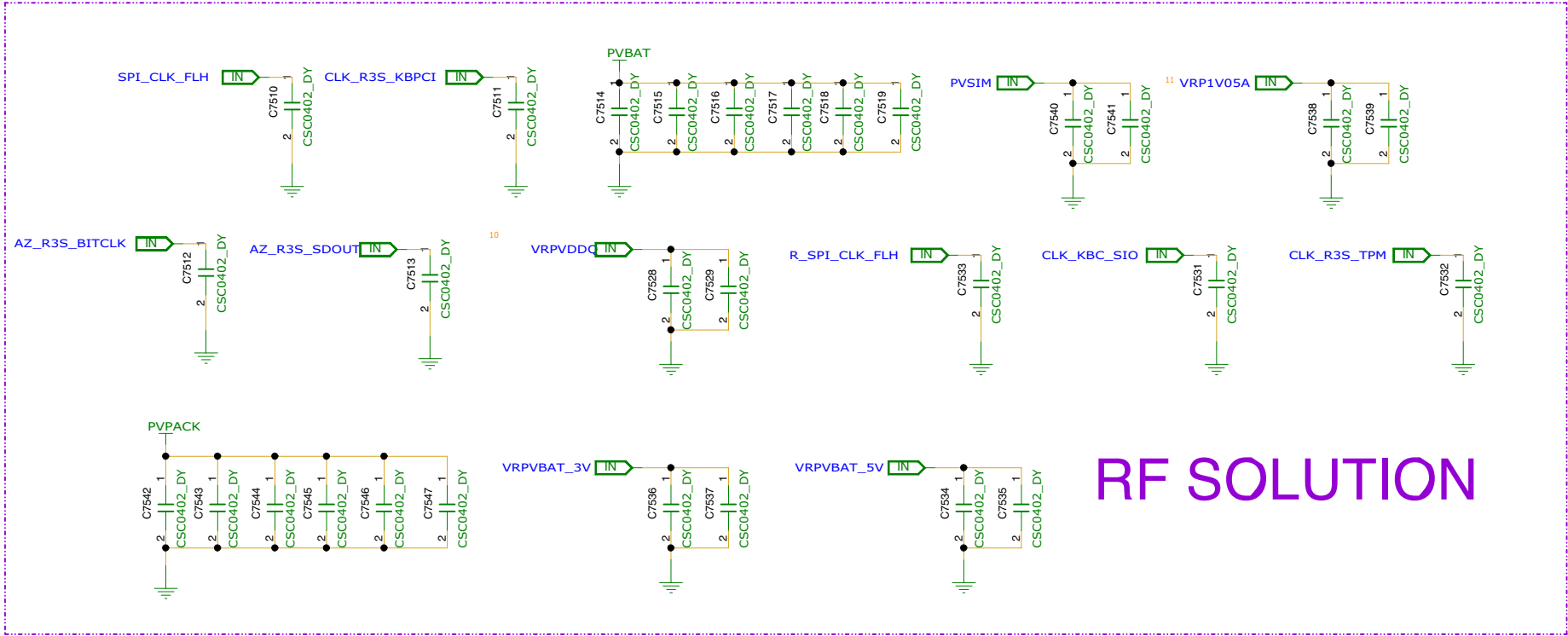
INVENTEC

TITLE  
MODEL PROJECT,FUNCTION  
SCREW

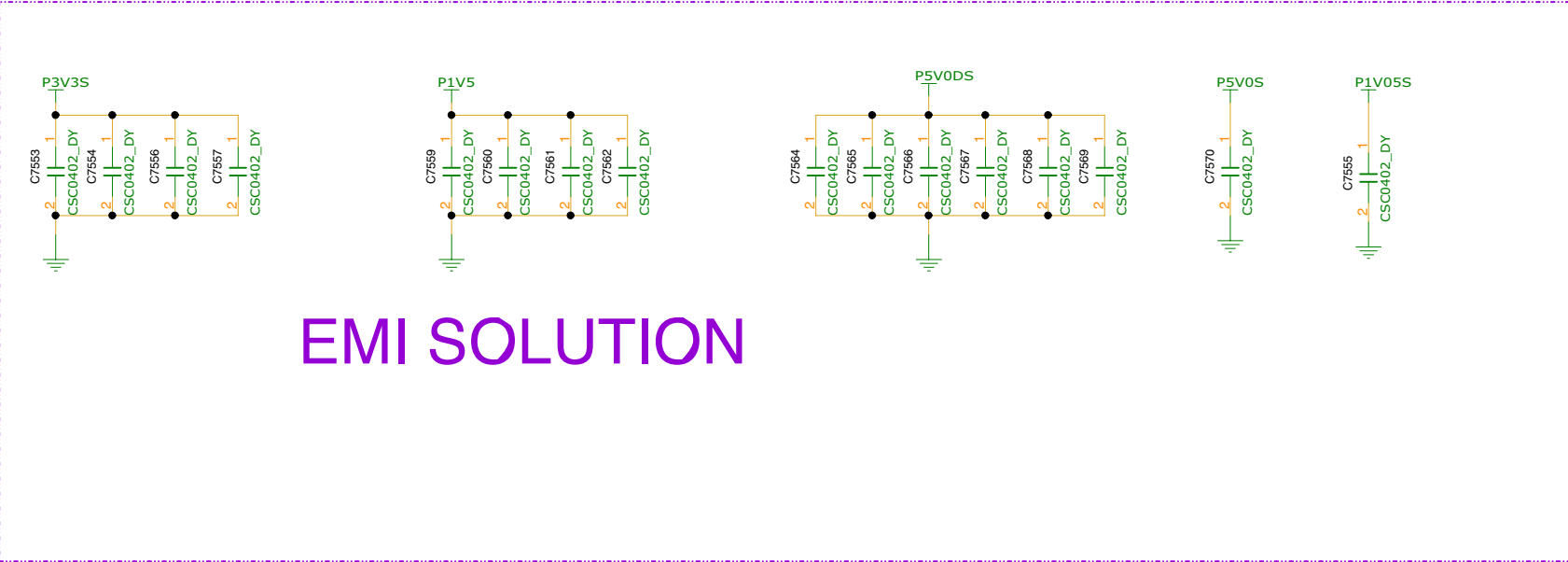
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

SHEET 66 of 77

CHANGE by XXX DATE 21-OCT-2002



# RF SOLUTION



# EMI SOLUTION

INVENTEC			
TITLE			
MODEL PROJECT FUNCTION			
EMI & RF SOLUTION			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET 67 of 77			

[illegible][illegible]

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

MLPS TABLE

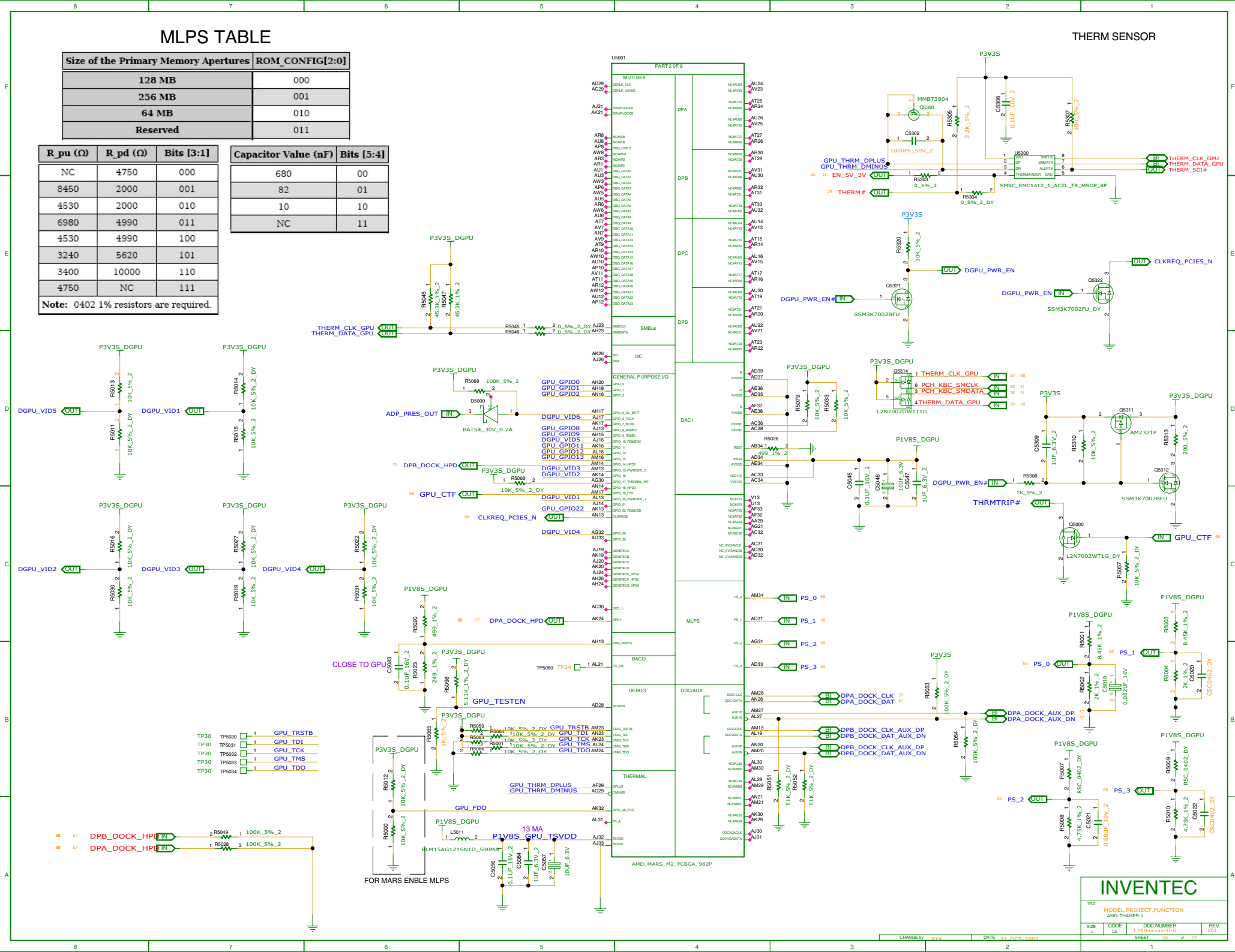
Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR



MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

**MLPS TABLE**

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

**Capacitor Value (nF) Bits [5:4]**

680	00
82	01
10	10
NC	11

**Note:** 0402 1% resistors are required.

**THERM SENSOR**

**INVENTEC**

FILE	MODEL/PROJECT/FUNCTION
AMD-THAMES-1	

SIZE	CODE	DOC NUMBER	REV
C	15	1310-000-01-01	01

CHANGE by: V.V.V. DATE: 24-01-2022

MLPS TABLE

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011

R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

THERM SENSOR

LPT-LP GPIO 34	MARS MLPS Bit: PS_3 [3:1]			R <sub>pu</sub> (Ω)	R <sub>pd</sub> (Ω)	Vendor & PN	Die Ver.	
0	0	0	0	NC	4750	Samsung - K4G20325FD-FC04	D	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	0	0	1	8450	2000	Hynix - H5GQ2H24AFR-T2C	A (Gemma)	GDDR5 - 64Mx32/128Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
1	1	1	0	3400	10000	*Samsung - K4G41325FC-HC04	C	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
	1	1	1	4759	NC	*Hynix - H5GC4H24MFR-T0C	Huma	*GDDR5 - 128Mx32/256Mx16, 1.5V/1.35V, 5.0Gbps/4Gbps
VBIOS selection :	Vram configuration			Vendor ID		Vram information		
0 : VBIOS 1, 64Mx32 for 1GB sku	00: 64Mx32 (2Gb)			0: Samsung		* 2GB sku, TBD		
1 : VBIOS 2, 128Mx32 for 2GB sku	11: 128Mx32 (4Gb)			1: Hynix				

### MLPS Implementation

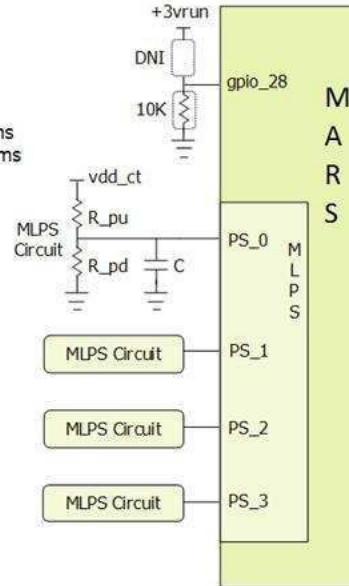
- Connect GPIO\_28 to 10K pulldown to enable MLPS
- If any of PS\_0/1/2/3 is not used, leave "no connect"
- R<sub>pu</sub>, R<sub>pd</sub> and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R <sub>pu</sub> (Ohm)	R <sub>pd</sub> (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111



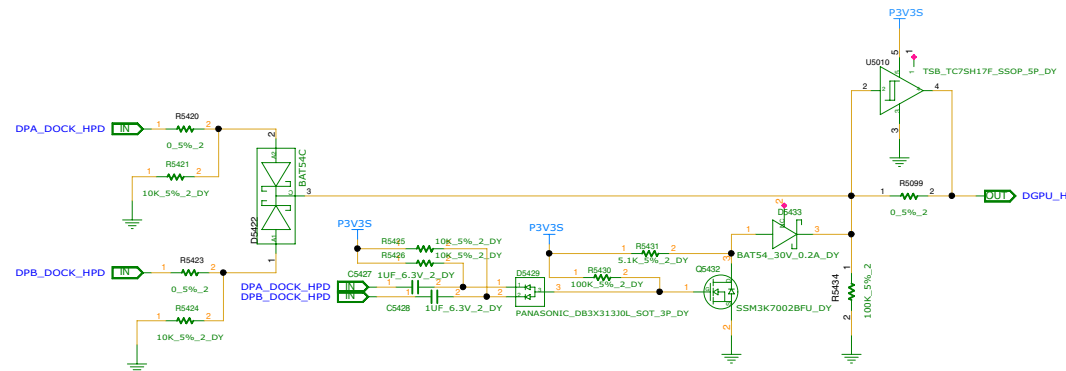
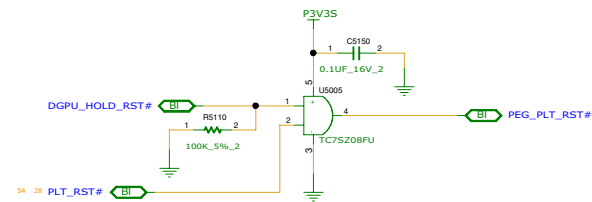
MLPS Bit	Strap Name	Description
PS_0[1]	ROM_CONFIG[0]	See Primary Memory Aperture Sizes.
PS_0[2]	ROM_CONFIG[1]	
PS_0[3]	ROM_CONFIG[2]	
PS_0[4]	N/A	Reserved for internal use only. <b>Must be 1 at reset.</b>
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap that indicates the number of audio-capable display outputs.
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. <b>1 = PCIe GEN3 is supported.</b>
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). <b>0 = The CLKREQB power management capability is disabled</b>
PS_1[3]	N/A	Reserved for internal use only. <b>Must be 0 at reset.</b>
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode <b>1 = The transmitter full-swing is enabled</b>
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. <b>1 = Tx deemphasis enabled.</b>
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. <b>0 = Disable the external BIOS ROM device.</b>
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). <b>0 = VGA controller capacity enabled.</b>
PS_2[5]	N/A	Reserved
PS_2[1]	N/A	Reserved.
PS_2[2]	N/A	Reserved.
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. <b>0 = Disable the external BIOS ROM device.</b>
PS_2[4]	STRAP_BIF_VGA_DIS	VGA disable determines whether or not the card will be recognized as the system's VGA controller (through the SUBCLASS field in the PCI configuration space). <b>0 = VGA controller capacity enabled.</b>
PS_2[5]	N/A	Reserved
PS_3[1]	BOARD_CONFIG[0]	See Board configuration related strapping, such as for memory ID.
PS_3[2]	BOARD_CONFIG[1]	
PS_3[3]	BOARD_CONFIG[2]	
PS_3[4]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user. 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.
PS_3[5]	AUD_PORT_CONN_PINSTRAP[2]	

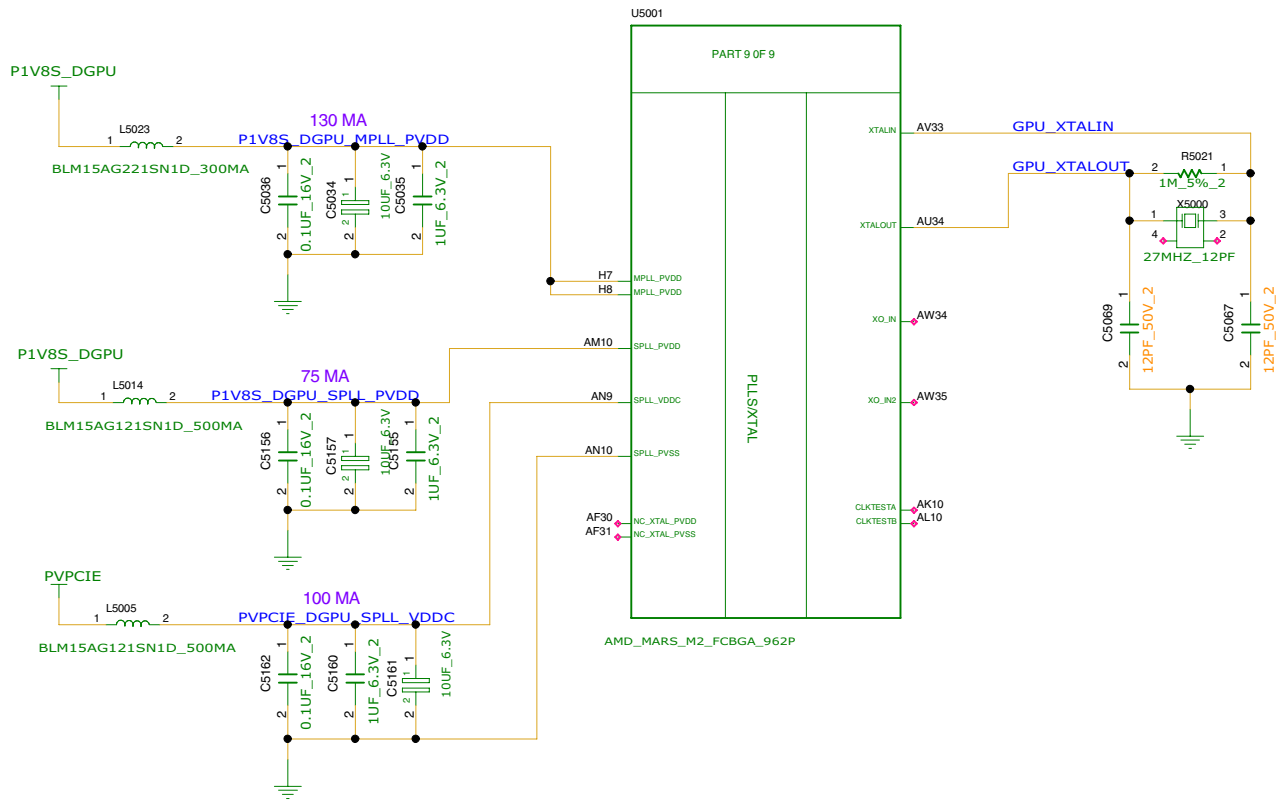
Note : AUD[1] (on HYSNC) and AUD[0] (on VSYNC) still need to be properly pin strapped even in a MLPS-based design.

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

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TITLE			
MODEL, PROJECT, FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310XXXX-0-0	201
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TITLE  
MODEL, PROJECT, FUNCTION  
Block Diagram

SIZE A3 CODE CS DOC NUMBER 1310xxxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 21 of 77











VM\_DQB0\_<31..0>

VM\_DQB1\_<31..0>

P1V35S\_DGPU

P1V35S\_DGPU

AMD\_MARS\_M2\_FCBGA\_962P

U5001

PART 4 OF 9

GDORS/DDR3

MEMORY INTERFACE B

MAB0\_0MAB\_0  
MAB0\_1MAB\_1  
MAB0\_2MAB\_2  
MAB0\_3MAB\_3  
MAB0\_4MAB\_4  
MAB0\_5MAB\_5  
MAB0\_6MAB\_6  
MAB0\_7MAB\_7  
MAB0\_8MAB\_8  
MAB1\_1MAB\_9  
MAB1\_2MAB\_10  
MAB1\_3MAB\_11  
MAB1\_4MAB\_12  
MAB1\_5BA2  
MAB1\_6BA0  
MAB1\_7BA1

WCKB0\_0DQMB\_0  
WCKB0B\_0DQMB\_1  
WCKB0\_1DQMB\_2  
WCKB0B\_1DQMB\_3  
WCKB1\_0DQMB\_4  
WCKB1B\_0DQMB\_5  
WCKB1\_1DQMB\_6  
WCKB1B\_1DQMB\_7

EDCB0\_0QSB\_0  
EDCB0\_1QSB\_1  
EDCB0\_2QSB\_2  
EDCB0\_3QSB\_3  
EDCB1\_0QSB\_4  
EDCB1\_1QSB\_5  
EDCB1\_2QSB\_6  
EDCB1\_3QSB\_7

DDIB0\_0QSB\_0B  
DDIB0\_1QSB\_1B  
DDIB0\_2QSB\_2B  
DDIB0\_3QSB\_3B  
DDIB1\_0QSB\_4B  
DDIB1\_1QSB\_5B  
DDIB1\_2QSB\_6B  
DDIB1\_3QSB\_7B

ADB0\_0DTB0  
ADB1\_0DTB1

CLKB0  
CLKB0B  
CLKB1  
CLKB1B

RASB0  
RASB1

CASB0  
CASB1

CSB0\_0  
CSB0B\_1

CSB1B\_0  
CSB1B\_1

CKEB0  
CKEB1

WEB0  
WEB1

MAB0\_8MAB\_13  
MAB1\_8MAB\_14  
MAB0\_9MAB\_15  
MAB1\_9RSVD

DRAM\_RST

AH11

R5080

R5041

C5174

120PF\_50V\_2

4.99K\_1%\_2

10\_5%\_2

51\_1%\_2

VM\_MAB0\_<7..0>

VM\_MAB1\_<7..0>

VM\_WCKB0\_0\_DP

VM\_WCKB0\_0\_DN

VM\_WCKB0\_1\_DP

VM\_WCKB0\_1\_DN

VM\_WCKB1\_0\_DP

VM\_WCKB1\_0\_DN

VM\_WCKB1\_1\_DP

VM\_WCKB1\_1\_DN

VM\_EDCB0\_0

VM\_EDCB0\_1

VM\_EDCB0\_2

VM\_EDCB0\_3

VM\_EDCB1\_0

VM\_EDCB1\_1

VM\_EDCB1\_2

VM\_EDCB1\_3

VM\_DDBIB0\_0

VM\_DDBIB0\_1

VM\_DDBIB0\_2

VM\_DDBIB0\_3

VM\_DDBIB1\_0

VM\_DDBIB1\_1

VM\_DDBIB1\_2

VM\_DDBIB1\_3

VM\_ADBIB0\_77

VM\_ADBIB1\_77

VM\_CLKB0\_DP

VM\_CLKB0\_DN

VM\_CLKB1\_DP

VM\_CLKB1\_DN

VM\_RASB0#

VM\_RASB1#

VM\_CASB0#

VM\_CASB1#

VM\_CSB0#\_0

VM\_CSB1#\_0

VM\_CKEB0\_77

VM\_CKEB1\_77

VM\_WEB0#

VM\_WEB1#

VM\_MAB0\_<8>

VM\_MAB1\_<8>

DRAM\_RST# 76 77

INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
AMD THAMES-3

SIZE A3  
CODE CS  
DOC NUMBER  
1310xxxx-0-0  
REV  
X01

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